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S540-15_NB8606_M/B Schematics Document

Intel WHL-U with DDR4 + N17S-G2

REV4.0

2019-01-02

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Reviewer	Nelosn.Hai & Nemo.Jiang	Page name: Cover page		
Approver	Lobo_Fan	Size: A4	Project Name: NB8606	REV: V4.0
		Date: Thursday, July 18, 2019	Sheet: 1	of 72

MEM ID

HW_ID0	HW_ID1	HW_ID2	Description	Total
0	0	0	NA	NA
1	0	0	4x Micron 8Gbx16 MT40A512M16LY-075:E	4GB
0	1	0	4x Hynix 8Gbx16 H5AN8G6NCJR-VKC	4GB
1	1	0	4x Samsung 8Gbx16 K4A8G165WC-BCTD	4GB
0	0	1	4x 16Gb(reserve)	8GB
1	0	1	4x 16Gb(reserve)	8GB
0	1	1	4x 16Gb(reserve)	8GB

GPU ID

HW_ID3	HW_ID4	Description
0	0	UMA
1	1	N17S-G2
0	1	GTX1150 Max-Q
1	0	Reserve

Phase ID

HW_ID5	HW_ID6	Description
0	1	EVT
1	0	FVT
1	1	SIT
0	0	SVT&SOVP

Reserve ID

HW_ID7	Description
0	Reserve
1	Reserve

BOM Option Table

Item	BOM Option
DDR4 Memory Down	DDR4_MD
Discrete GPU Stuff	GPU
DGPU Serial Select	N16@/N17@
Not Stuff	ns
DDR4 Memory Down 4GB Group	DDR4_4G@
VRAM GDDR5 2GB Group	GDDR5_2GB@
GPU ID Select	GPU_ID
On board memory ID Select	Memory_ID
Finger Print component	FP

Voltage Rails

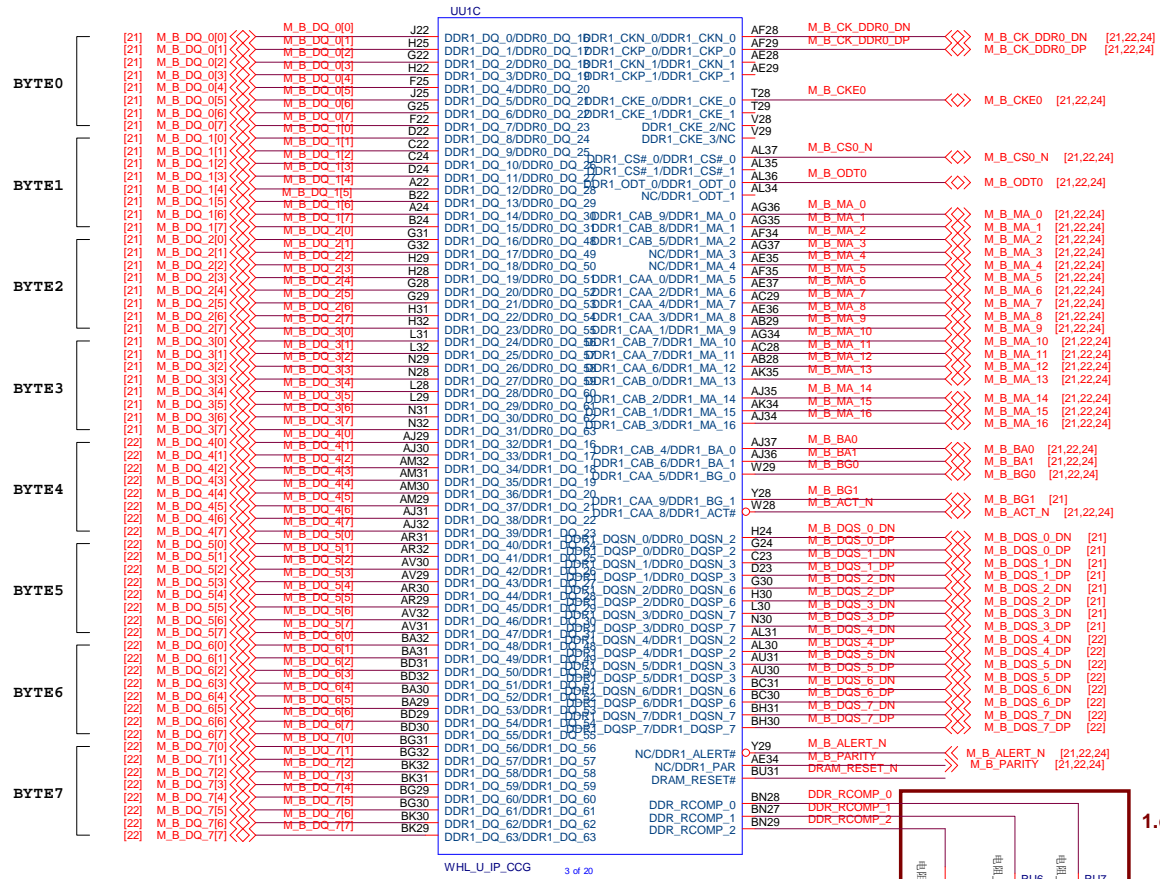
Power Plane	Description	S0	S3	S4/S5
+VBAT	Battery power supply	ON	ON	ON
+VSYS	AC or battery power rail for system	ON	ON	ON
+VCC3P3_LDO_OUT	3.3V LDO power rail	ON	ON	ON
+VCCRTC	Power supply for RTC	ON	ON	ON
+V5P0A	+5V Always power rail	ON	ON	ON
+V3P3A	+3.3V Always power rail	ON	ON	ON
+V1P8A	+1.8V Always power rail	ON	ON	ON
+V1P05A	+1.05V Always power rail	ON	ON	ON
+V1P2U_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF
+V2P5U_VPP	DDR4 activating power supply	ON	ON	OFF
+VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF
+V5P0SX	System +5V power rail	ON	OFF	OFF
+V3P3SX	System +3.3V power rail	ON	OFF	OFF
+V1P8SX	System +1.8V power rail	ON	OFF	OFF
+VCCSTG_IO	CPU IO power rail	ON	OFF	OFF
+V_VDDQ_VTT	DDR +0.6V power rail for DDR terminator	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+V1P8_V3P3_AON	+3.3V for N16/ +1.8V power rail for N17S(AON)	ON*1	OFF	OFF
+V1P8_V3P3_MAIN	+3.3V for N16/ +1.8V power rail for N17S(MAIN)	ON*1	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON*1	OFF	OFF
+1.0VGS	+1.05V for N16/ +1.0V power rail for N17S	ON*1	OFF	OFF
+1.35VGS	+1.35V power rail for GPU	ON*1	OFF	OFF

Note: 1.Above voltage rails are based AC mode.
2.ON*1 power rail is ON when DGPU is turned on.

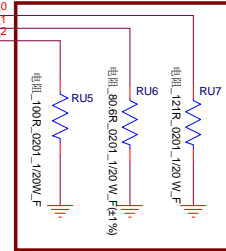
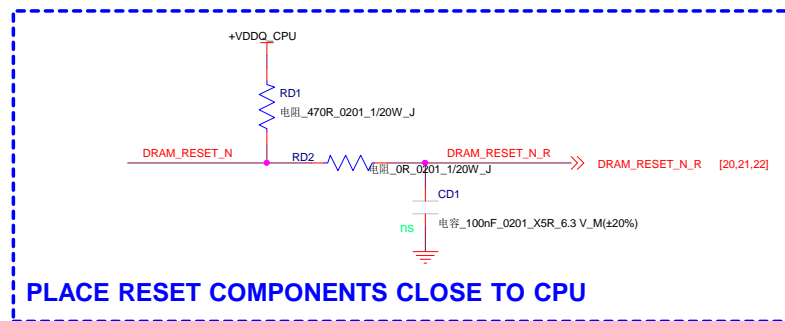
2



CHB_MD



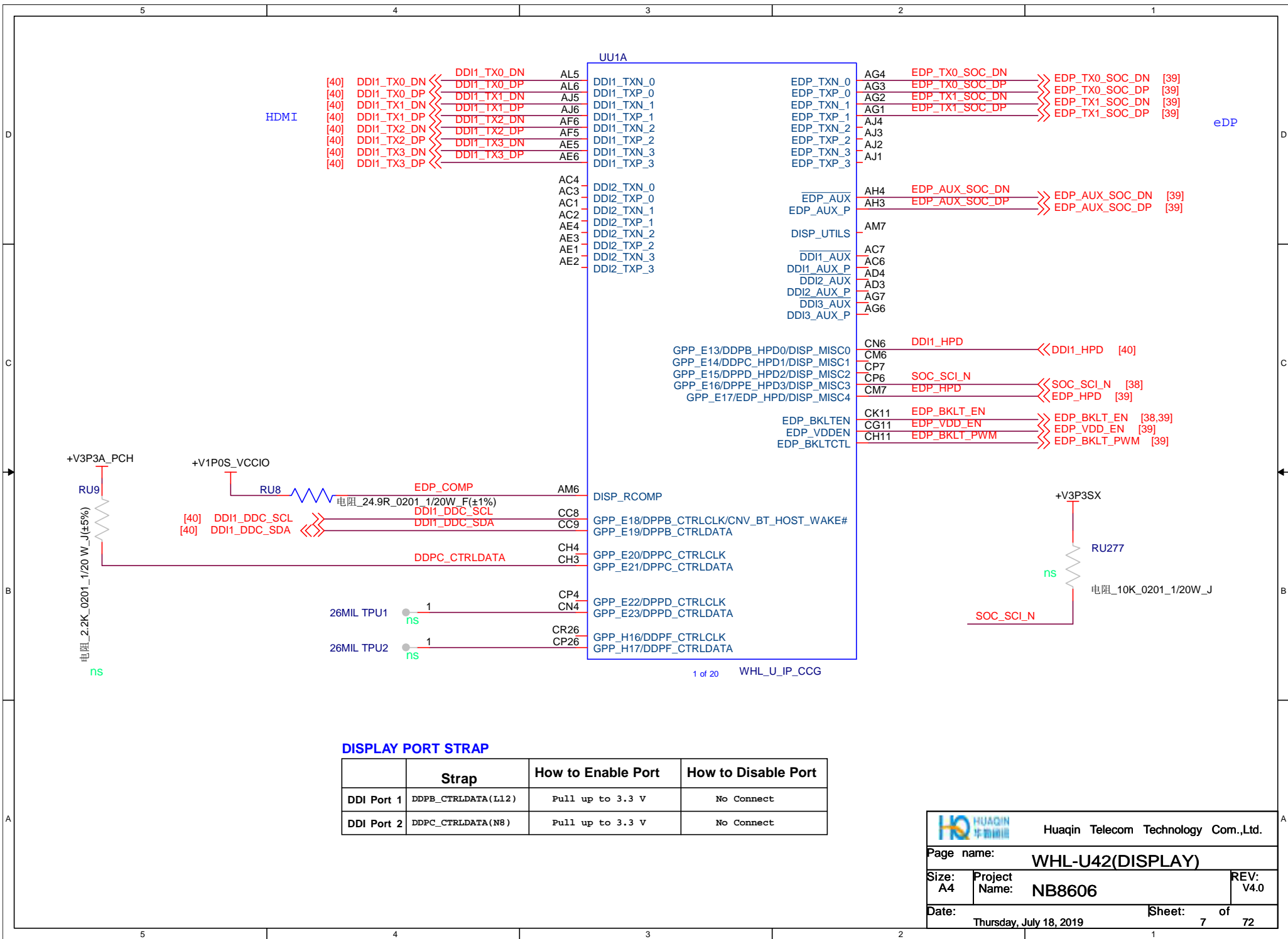
1.change RU7 to 121Ω 2018 06 06



BOM NOTE


CFL-U43e/WHLU42:
[0]:121
[1]:80.6
[2]:100
CNL-U22:
100/100/100

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DISPLAY PORT STRAP

	Strap	How to Enable Port	How to Disable Port
DDI Port 1	DDPB_CTRLDATA(L12)	Pull up to 3.3 V	No Connect
DDI Port 2	DDPC_CTRLDATA(N8)	Pull up to 3.3 V	No Connect

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Page name:

WHL-U42(DISPLAY)

Size: A4

Project Name:

NB8606

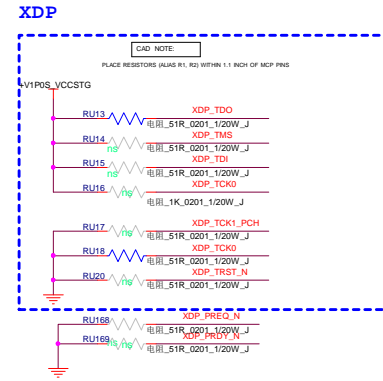
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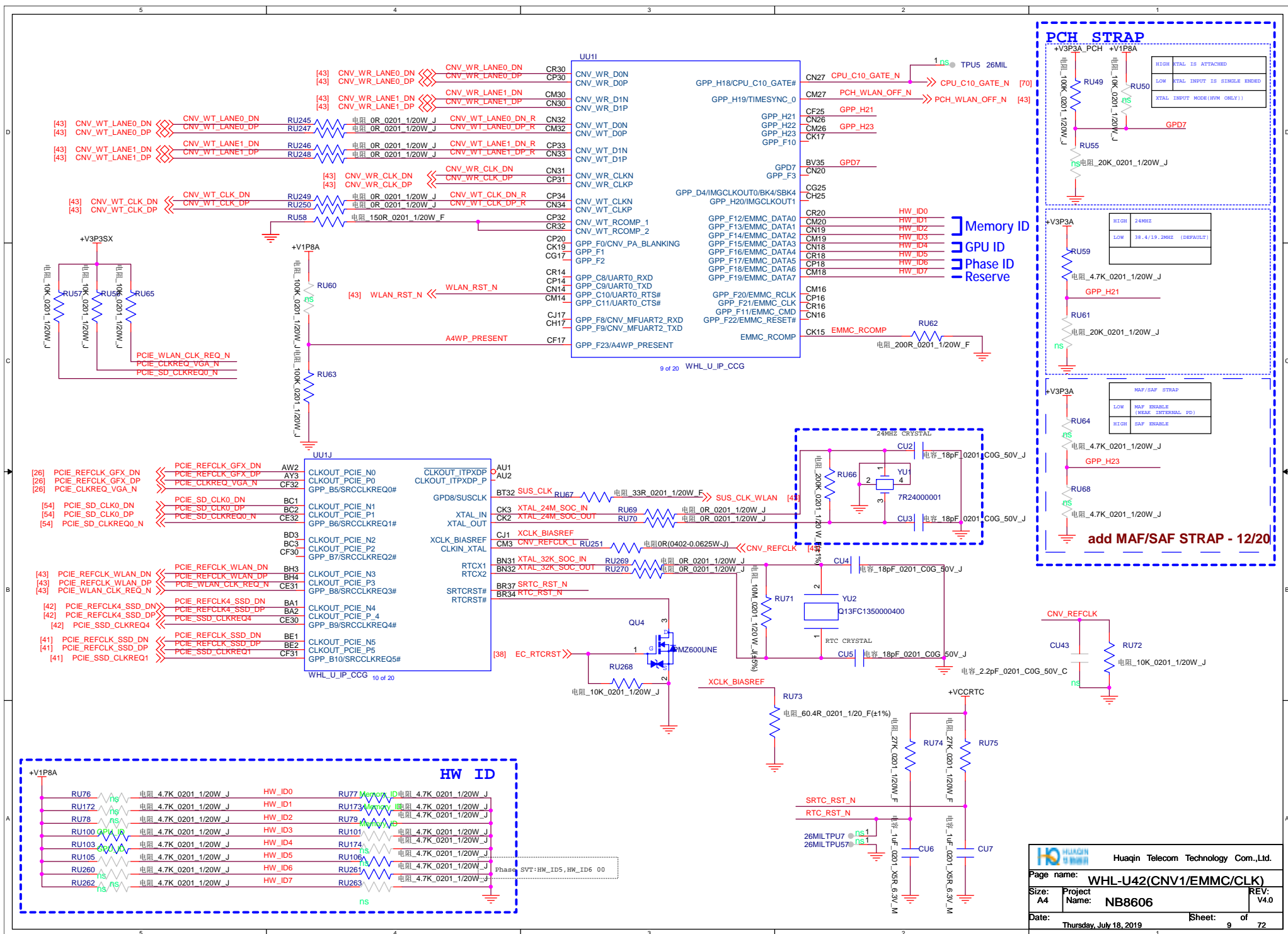
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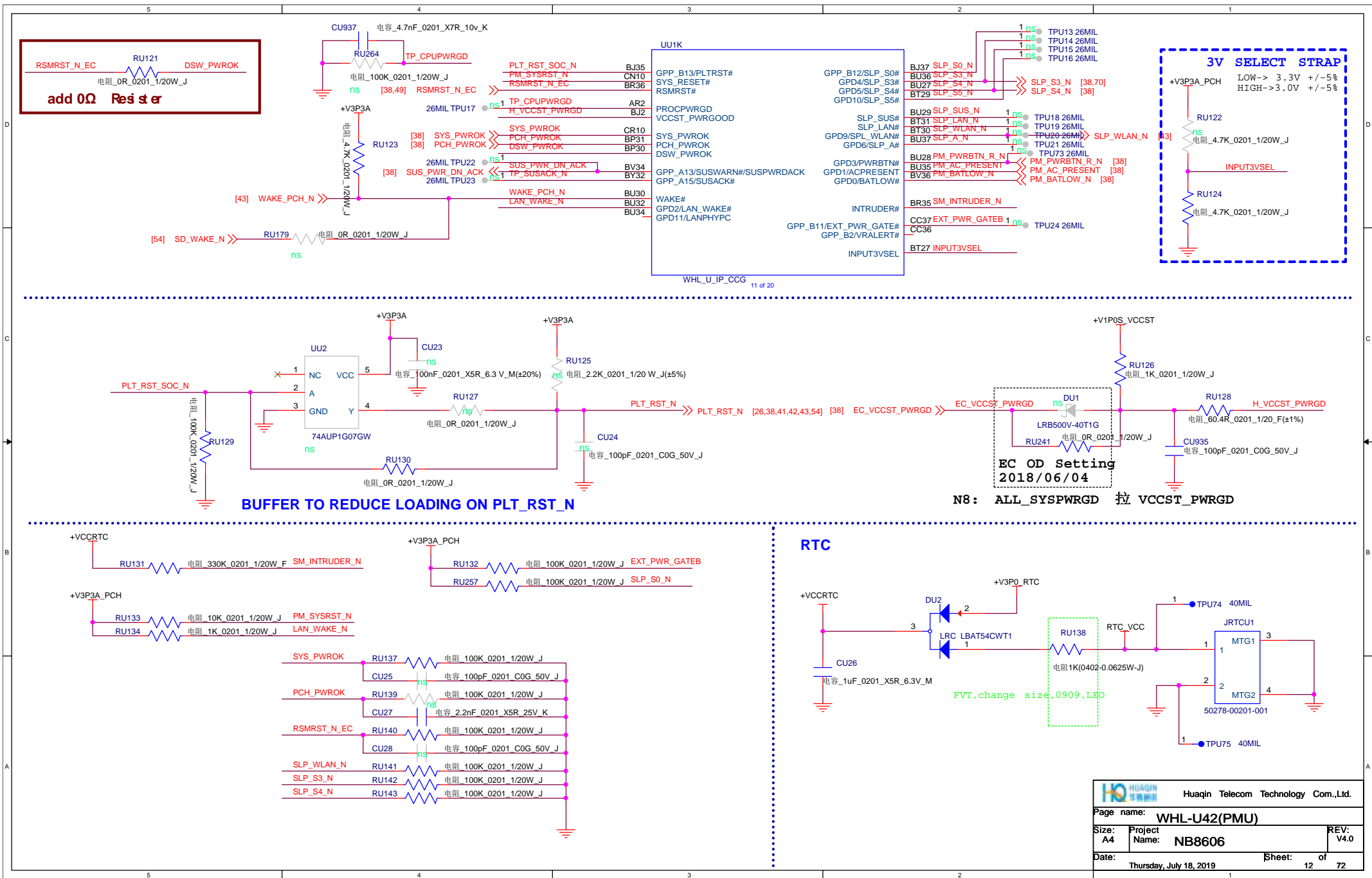
Thursday, July 18, 2019

Sheet:

7 of 72







+VCC_CORE

+VCC_CORE

UU1L

AN9 VCCCORE_28 VCCCORE_67
AN24 VCCCORE_29 VCCCORE_68
AN26 VCCCORE_30 VCCCORE_69
AN27 VCCCORE_31 VCCCORE_70
AP2 VCCCORE_32 VCCCORE_71
AP9 VCCCORE_33 VCCCORE_72
AP9 VCCCORE_34 VCCCORE_73
AP24 VCCCORE_35 VCCCORE_74
AP26 VCCCORE_36 VCCCORE_75
AR5 VCCCORE_37 VCCCORE_76
AR6 VCCCORE_38 VCCCORE_77
AR7 VCCCORE_39 VCCCORE_78
AR8 VCCCORE_40 VCCCORE_79
AR10 VCCCORE_41 VCCCORE_80
AR25 VCCCORE_42 VCCCORE_81
AR27 VCCCORE_43 VCCCORE_82
AT9 VCCCORE_44 VCCCORE_83
AT24 VCCCORE_45 VCCCORE_84
AU5 VCCCORE_46 VCCCORE_85
AU6 VCCCORE_47 VCCCORE_86
AU7 VCCCORE_48 VCCCORE_87
AU8 VCCCORE_49 VCCCORE_88
AU9 VCCCORE_50 VCCCORE_89
AU24 VCCCORE_51 VCCCORE_90
AU25 VCCCORE_52 VCCCORE_91
AU26 VCCCORE_53 VCCCORE_92
AU27 VCCCORE_54 VCCCORE_93
AV2 VCCCORE_55 VCCCORE_94
AV5 VCCCORE_56 VCCCORE_95
AV7 VCCCORE_57 VCCCORE_96
AV10 VCCCORE_58 VCCCORE_97
AV27 VCCCORE_59 VCCCORE_98
AV5 VCCCORE_60 VCCCORE_99
AW5 VCCCORE_61 VCCCORE_100
AW7 VCCCORE_62 VCCCORE_101
AW8 VCCCORE_63
AW9 VCCCORE_64
AW10 VCCCORE_65
AW11 VCCCORE_66

VCC SENSE

VSS SENSE

VIDALERT#

VIDSCK

VIDSOUT

RSVD_65

VCCSTG_3

12 of 20WHL_U_IP_CCG

note:
Only ES2

CAD NOTE:
PLACE THE PU RESISTOR
CLOSE TO CPU

+VCC_GT

UU1M

WHL_QS/CFU/WHL_ES1_CNL_U

A5 VCCGT_1
A6 VCCGT_2
A8 VCCGT_3
A11 VCCGT_4
A12 VCCGT_5
A14 VCCGT_6
A15 VCCGT_7
A17 VCCGT_8
A18 VCCGT_9
A20 VCCGT_10
B3 VCCGT_11
B4 VCCGT_12
B6 VCCGT_13
B8 VCCGT_14
B11 VCCGT_15
B14 VCCGT_16
B17 VCCGT_17
B20 VCCGT_18
C2 VCCGT_19
C3 VCCGT_20
C6 VCCGT_21
C7 VCCGT_22
C8 VCCGT_23
C11 VCCGT_24
C12 VCCGT_25
C14 VCCGT_26
C15 VCCGT_27
C17 VCCGT_28
C18 VCCGT_29
D4 VCCGT_30
D7 VCCGT_31
D11 VCCGT_32
D12 VCCGT_33
D14 VCCGT_34
D15 VCCGT_35
D17 VCCGT_36
D18 VCCGT_37
D20 VCCGT_38
E4 VCCGT_39
F5 VCCGT_40
F6 VCCGT_41
F7 VCCGT_42
F8 VCCGT_43
F11 VCCGT_44
F14 VCCGT_45
F20 VCCGT_46
G11 VCCGT_47
G12 VCCGT_48
G14 VCCGT_49
G15 VCCGT_50
G17 VCCGT_51
G18 VCCGT_52
G20 VCCGT_53
H5 VCCGT_54
H6 VCCGT_55
H7 VCCGT_56
H8 VCCGT_57
H9 VCCGT_58
H11 VCCGT_59
H12 VCCGT_60
H14 VCCGT_61
H15 VCCGT_62
H17 VCCGT_63
H18 VCCGT_64
H20 VCCGT_65
J7 VCCGT_66
J8 VCCGT_67
J11 VCCGT_68
J14 VCCGT_69
J17 VCCGT_70
J20 VCCGT_71
K2 VCCGT_72
K11 VCCGT_73
L7 VCCGT_74
L8 VCCGT_75
L10 VCCGT_76
M9 VCCGT_77
N7 VCCGT_78
N8 VCCGT_79
N9 VCCGT_80
N10 VCCGT_81
P2 VCCGT_82
P8 VCCGT_83
R9 VCCGT_84
T8 VCCGT_85
T9 VCCGT_86
T10 VCCGT_87
U8 VCCGT_88
U10 VCCGT_89
V9 VCCGT_90
W8 VCCGT_91
W9 VCCGT_92
AA9 VCCGT_93
AB2 VCCGT_94
AB8 VCCGT_95
AB9 VCCGT_96
AB10 VCCGT_97
AC8 VCCGT_98
AD9 VCCGT_99
AE8 VCCGT_100
AE9 VCCGT_101
AE10 VCCGT_102
AF2 VCCGT_103
AF8 VCCGT_104
AF10 VCCGT_105
AG5 VCCGT_106
AG9 VCCGT_107
AH9 VCCGT_108
AJ8 VCCGT_109
AJ10 VCCGT_110
AK2 VCCGT_111
AK9 VCCGT_112
AL8 VCCGT_113
AL9 VCCGT_114
AL10 VCCGT_115
AM8 VCCGT_116
V2 VCCGT_117
Y8 VCCGT_118
Y10 VCCGT_119

13 of 20 WHL_U_IP_CCG

+VCC_GT

31A Max

+VCC_CORE

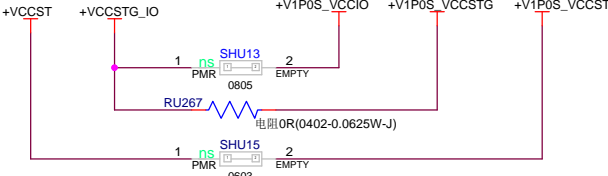
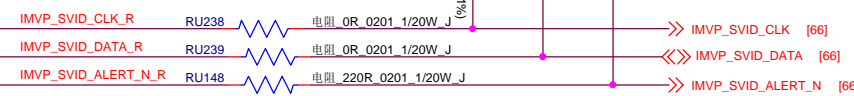
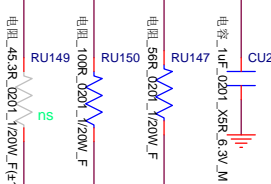
70A Max

E3 VCCGT_SNS_P
D2 VCCGT_SNS_N

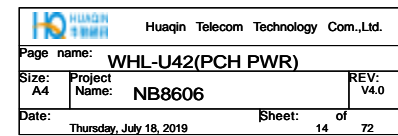
VCCGT_SNS_P [66]
VCCGT_SNS_N [66]

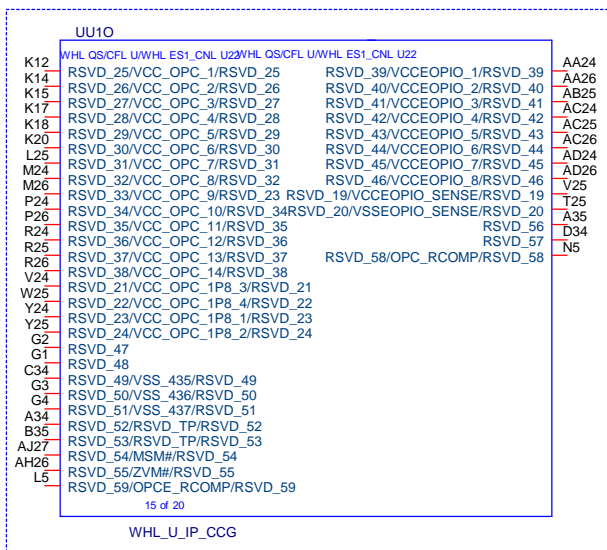
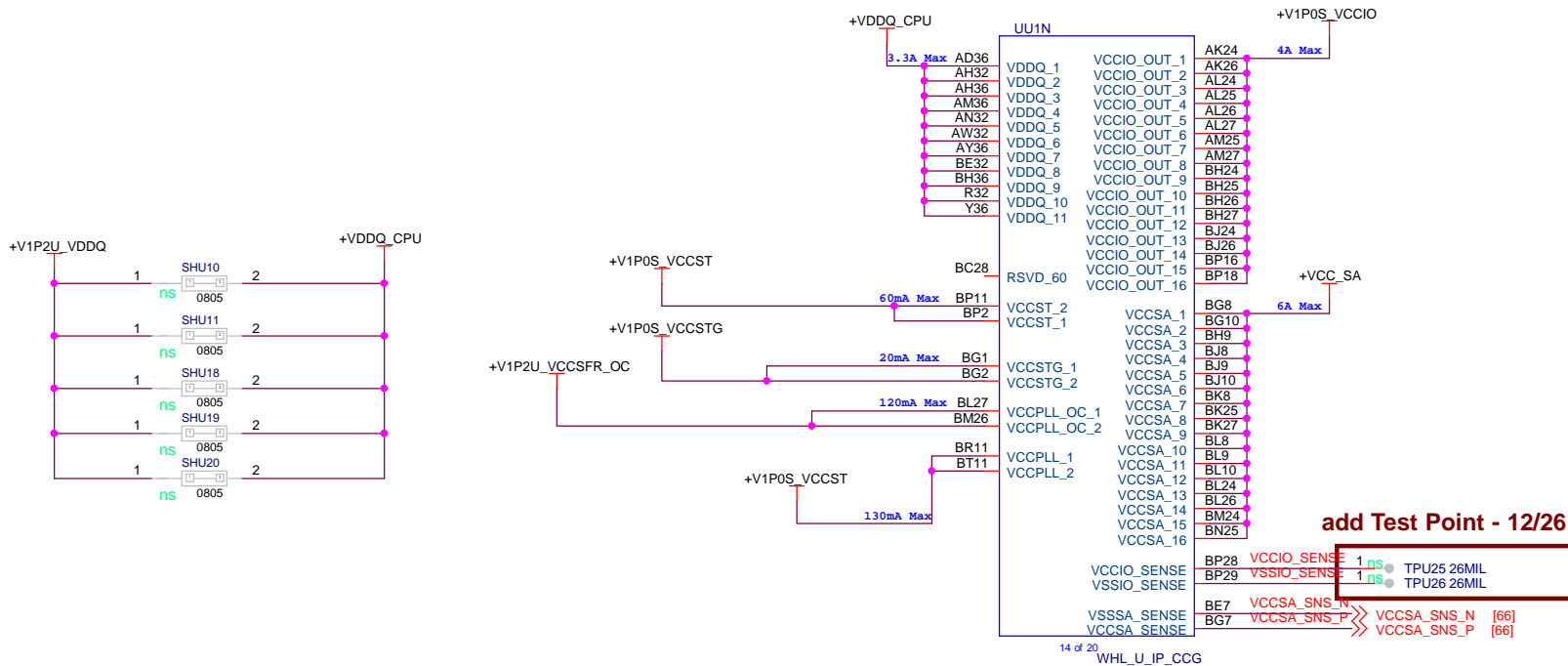
CLOSE TO CPU

+V1P0S_VCCST



Huaqin Telecom Technology Com., Ltd.	
Page name: WHL-U42(VCORE/GT)	
Size: A4	Project Name: NB8606
Date: Thursday, July 18, 2019	Sheet: 13 of 72





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UU1R			
CR34			BL7
BT5	VSS_342	VSS_330	AE25
BY6	VSS_351	VSS_337	BM33
CP35	VSS_361	VSS_345	CM5
CS37	VSS_371	VSS_354	AE27
CK37	VSS_381	VSS_364	BM35
AW11	VSS_391	VSS_374	CM6
CM1	VSS_401	VSS_384	AE30
BD6	VSS_411	VSS_302	BM36
AY4	VSS_421	VSS_308	CN13
B34	VSS_360	VSS_315	AE7
F35	VSS_370	VSS_322	BM9
A4	VSS_380	VSS_329	CN17
AE24	VSS_390	VSS_336	AF27
AE26	VSS_400	VSS_344	BN30
AF25	VSS_410	VSS_353	CN21
AG24	VSS_420	VSS_363	AF3
AG26	VSS_428	VSS_373	BN7
AH24	VSS_434	VSS_295	CN25
AH25	VSS_296	VSS_301	AF30
B2	VSS_350	VSS_307	CN29
B36	VSS_359	VSS_314	AF33
C36	VSS_369	VSS_321	BP15
C37	VSS_379	VSS_328	AF36
CN1	VSS_389	VSS_335	AF4
CN2	VSS_399	VSS_343	CN5
CN37	VSS_409	VSS_352	AF7
CP2	VSS_419	VSS_362	BP25
D1	VSS_427	VSS_416	CN9
A32	VSS_433	VSS_425	AG10
F33	VSS_341	VSS_432	BP3
A3	VSS_349	VSS_294	CP1
BJ7	VSS_358	VSS_300	BP32
CJ36	VSS_368	VSS_306	CP11
A36	VSS_378	VSS_313	AH27
BK10	VSS_388	VSS_320	BP33
CJ4	VSS_398	VSS_327	CP13
AB27	VSS_408	VSS_334	AH28
BK2	VSS_418	VSS_405	BP4
CK1	VSS_426	VSS_415	CP15
AB3	VSS_333	VSS_424	AH29
BK28	VSS_340	VSS_431	BP7
AB30	VSS_348	VSS_293	CP19
BK3	VSS_357	VSS_299	AH30
CK4	VSS_367	VSS_305	CP21
AB33	VSS_377	VSS_312	AH31
BK33	VSS_387	VSS_319	BR19
CK7	VSS_397	VSS_326	CP27
AB36	VSS_407	VSS_394	AH33
BK4	VSS_417	VSS_404	BR25
CL2	VSS_325	VSS_414	AH35
AB4	VSS_332	VSS_423	CP37
BK7	VSS_339	VSS_430	AJ25
CM13	VSS_347	VSS_292	BT15
AB7	VSS_356	VSS_298	AJ28
BL25	VSS_366	VSS_304	BT16
CM17	VSS_376	VSS_311	CP9
AC10	VSS_386	VSS_318	AJ7
BL28	VSS_396	VSS_383	CR2
CM21	VSS_406	VSS_393	AK3
AC27	VSS_317	VSS_403	CR36
BL29	VSS_324	VSS_413	AK33
CM25	VSS_331	VSS_422	D21
AC30	VSS_338	VSS_429	AK36
BL30	VSS_346	VSS_291	BT25
CM29	VSS_355	VSS_297	D25
BL31	VSS_365	VSS_303	AK4
CM31	VSS_375	VSS_310	BT28
AD33	VSS_385	VSS_372	AL28
BL32	VSS_395	VSS_382	BT33
CM33	VSS_309	VSS_392	D5
AD35	VSS_316	VSS_402	AL29
	VSS_323	VSS_412	

17 of 20

WHL_U_IP_CCG

UU1S			
BT35			BY25
D6	VSS_277	VSS_180	J18
AL32	VSS_290	VSS_183	AU32
BT36	VSS_156	VSS_186	BY28
D8	VSS_172	VSS_257	J21
AL7	VSS_208	VSS_270	AV25
D9	VSS_217	VSS_284	J24
AM10	VSS_227	VSS_151	AV28
BU11	VSS_238	VSS_161	BY35
E23	VSS_250	VSS_169	J33
AM26	VSS_263	VSS_175	AV3
E27	VSS_276	VSS_179	BY36
AM33	VSS_289	VSS_182	J36
BU23	VSS_155	VSS_233	AV33
E29	VSS_164	VSS_244	J6
AM35	VSS_200	VSS_256	AV36
BU24	VSS_207	VSS_269	C1
E31	VSS_216	VSS_283	K21
BU25	VSS_226	VSS_150	AV4
E33	VSS_237	VSS_160	C21
AN25	VSS_249	VSS_168	K22
BU7	VSS_262	VSS_174	AV6
E9	VSS_275	VSS_178	C25
AN28	VSS_288	VSS_222	K24
BN11	VSS_154	VSS_232	AV6
F12	VSS_194	VSS_243	C29
AN29	VSS_199	VSS_255	K25
F15	VSS_206	VSS_268	AW28
AN30	VSS_215	VSS_282	C33
F18	VSS_225	VSS_149	K27
AN31	VSS_236	VSS_159	AW29
BU3	VSS_248	VSS_167	C4
F2	VSS_261	VSS_173	K28
AN7	VSS_274	VSS_212	AW3
BV31	VSS_287	VSS_221	C9
F21	VSS_189	VSS_231	K29
AN8	VSS_193	VSS_242	AW30
BV33	VSS_198	VSS_254	CA11
F24	VSS_205	VSS_267	K3
BV4	VSS_214	VSS_281	AW31
F3	VSS_224	VSS_148	CA15
AP3	VSS_235	VSS_158	K30
BW11	VSS_247	VSS_166	AY33
F4	VSS_260	VSS_203	CA22
AP33	VSS_273	VSS_211	K31
BW15	VSS_185	VSS_220	AY35
G21	VSS_188	VSS_230	K32
AP36	VSS_192	VSS_241	B12
G27	VSS_197	VSS_253	K4
AP4	VSS_204	VSS_266	B15
G33	VSS_213	VSS_280	CA25
AR28	VSS_223	VSS_147	K9
G35	VSS_234	VSS_157	B18
G36	VSS_246	VSS_196	CB11
AT33	VSS_259	VSS_202	L27
BW24	VSS_272	VSS_210	B21
G9	VSS_286	VSS_219	L33
AT35	VSS_153	VSS_229	B23
H21	VSS_163	VSS_240	L35
AT36	VSS_171	VSS_252	B25
BW7	VSS_177	VSS_265	CB18
H27	VSS_181	VSS_279	L36
AT4	VSS_184	VSS_146	B27
BY11	VSS_187	VSS_190	CB19
AU10	VSS_191	VSS_195	L6
BY15	VSS_258	VSS_201	B29
H9	VSS_271	VSS_209	CB2
AU28	VSS_285	VSS_218	N25
BY22	VSS_152	VSS_228	B31
J12	VSS_162	VSS_239	CB20
AD29	VSS_170	VSS_251	N27
J15	VSS_176	VSS_264	CB25
		VSS_278	

18 of 20

WHL_U_IP_CCG

UU1T			
N6			CF23
B37	VSS_66	VSS_99	V4
CB3	VSS_73	VSS_106	BE30
P10	VSS_79	VSS_115	CF28
B5	VSS_84	VSS_126	W10
CB33	VSS_89	VSS_139	BE31
P3	VSS_95	VSS_8	CF3
B7	VSS_102	VSS_19	W27
CB4	VSS_110	VSS_29	CF4
P33	VSS_120	VSS_83	W30
B9	VSS_132	VSS_87	BF3
CB7	VSS_145	VSS_92	CG33
P36	VSS_14	VSS_98	W7
BA10	VSS_25	VSS_105	BF33
CC11	VSS_35	VSS_114	CG7
P4	VSS_44	VSS_125	BF36
BA28	VSS_52	VSS_138	Y26
P7	VSS_59	VSS_16	BF4
BA3	VSS_65	VSS_18	CH31
CC20	VSS_72	VSS_77	Y27
R27	VSS_78	VSS_82	BG25
BB3	VSS_131	VSS_86	Y30
CC25	VSS_144	VSS_91	BG28
R28	VSS_13	VSS_97	CJ11
BB33	VSS_24	VSS_104	Y33
CC28	VSS_34	VSS_113	CJ14
R29	VSS_43	VSS_124	Y35
BB36	VSS_51	VSS_137	BH28
CC31	VSS_58	VSS_6	CJ19
R30	VSS_64	VSS_70	Y7
BB4	VSS_71	VSS_76	BH29
CC7	VSS_119	VSS_81	CJ23
R31	VSS_130	VSS_85	BH32
BC25	VSS_143	VSS_90	CJ28
CD11	VSS_12	VSS_96	BH33
T27	VSS_23	VSS_103	CJ33
CD12	VSS_33	VSS_112	BH35
T30	VSS_42	VSS_123	CJ35
BC29	VSS_50	VSS_136	BP19
CD14	VSS_57	VSS_5	BR16
T33	VSS_63	VSS_17	BY18
T35	VSS_109	VSS_28	BY19
BC32	VSS_118	VSS_38	CC16
CD24	VSS_129	VSS_47	BU16
T36	VSS_142	VSS_55	CC14
CD25	VSS_11	VSS_62	BR22
T7	VSS_22	VSS_69	BU20
OE33	VSS_32	VSS_75	CD20
BC8	VSS_41	VSS_80	BT14
U26	VSS_49	VSS_135	BP12
BD28	VSS_56	VSS_4	CB24
CE35	VSS_101	VSS_16	CC24
U7	VSS_108	VSS_27	J5
BD33	VSS_117	VSS_37	U24
CE36	VSS_128	VSS_46	BD7
V26	VSS_141	VSS_54	AR4
BD35	VSS_10	VSS_61	AJ4
CE7	VSS_21	VSS_68	AW4
V27	VSS_31	VSS_74	BA6
BD36	VSS_40	VSS_122	BC4
CF11	VSS_48	VSS_134	BE4
V3	VSS_94	VSS_3	BE8
BE10	VSS_100	VSS_15	BA4
CF14	VSS_107	VSS_26	BD4
V30	VSS_116	VSS_36	BG4
BE28	VSS_127	VSS_45	CJ2
CF19	VSS_140	VSS_53	CJ3
V33	VSS_9	VSS_60	AM5
BE29	VSS_20	VSS_67	CM4
CF2	VSS_30	VSS_111	AC5
V36	VSS_39	VSS_121	AG5
BE3	VSS_88	VSS_133	CR6
	VSS_93	VSS_2	

19 of 20
WHL_U_IP_CCG

+VCC_CORE

PLACE THESE CAPS UNDERNEATH BGA AREA

+VCCCORE

+VCC_GT

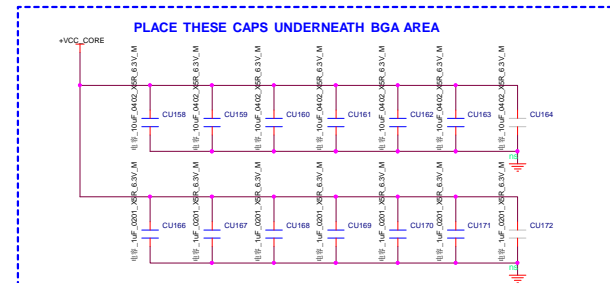
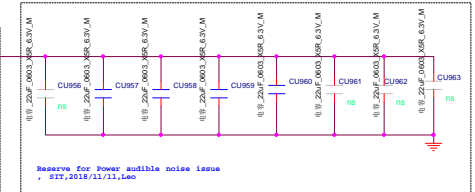
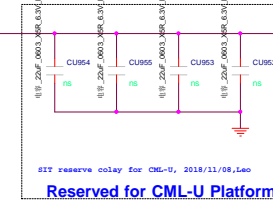
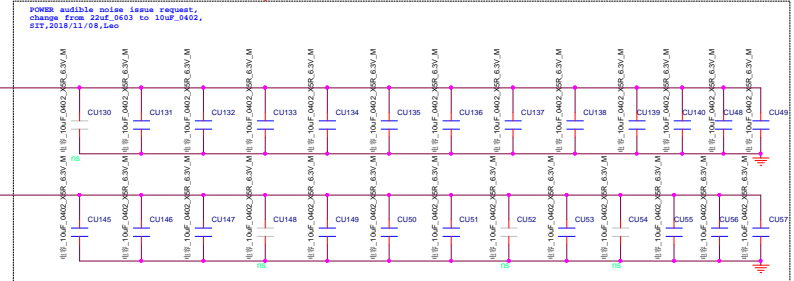
+VCCGT

PDG:15 x 10uF
11 x 1uF
15 x 22uF
8 x 47uF
7x(0603)
2x(0805)
VENDOR:26x 22uF-->11X1uF+26x 22uF

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PDG:35 x 1uF
22 x 10uF
9x 22uF
18x 47uF

VENDOR:33x 22uF-->35 X1uF+30X22uF+7X10uF

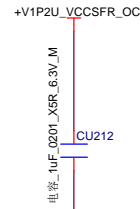
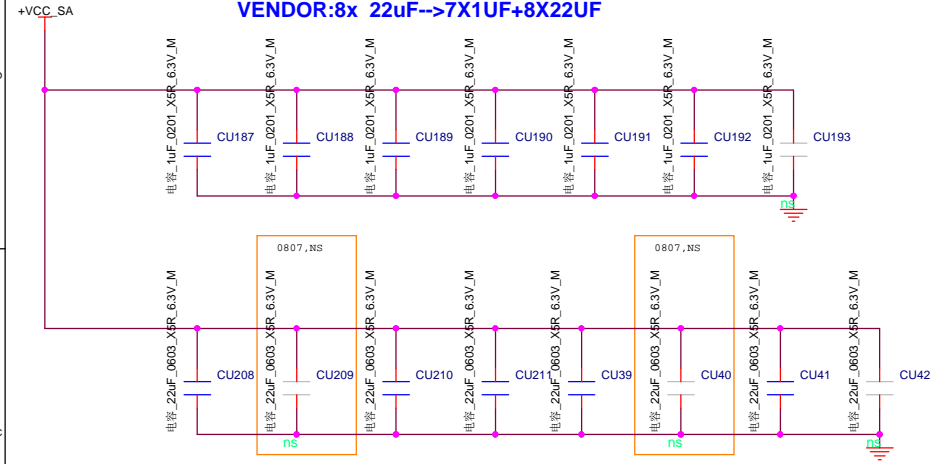


7 x 10uF
7 x 1uF

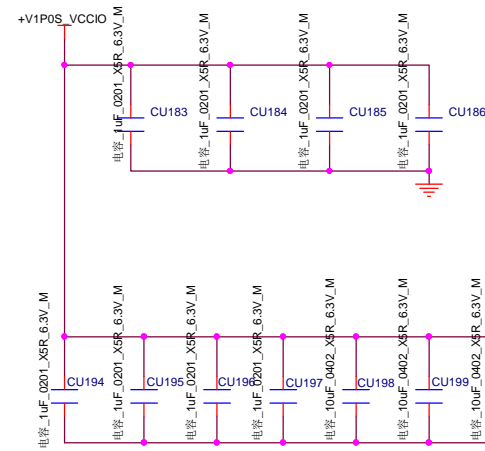
+VCCEPIO delete

PDG:7x 1uF
15X 10uF
2 x 47 uF
2 x (0805)

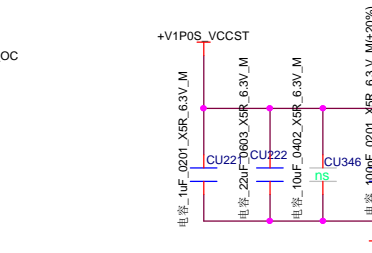
VENDOR:8x 22uF-->7X1UF+8X22UF



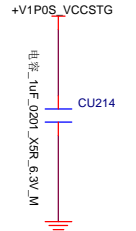
VCCPLL-OC 1x1uf



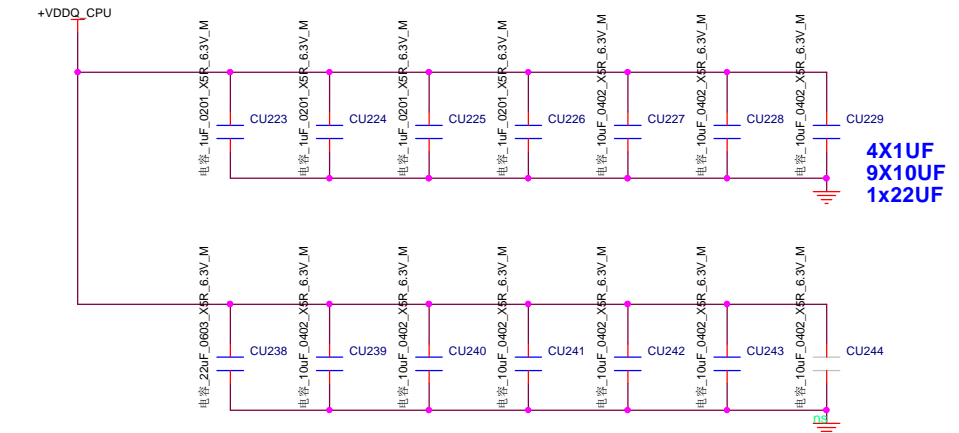
VCCPLL 1x1uf,1X0.1,2X(0402 10uF)



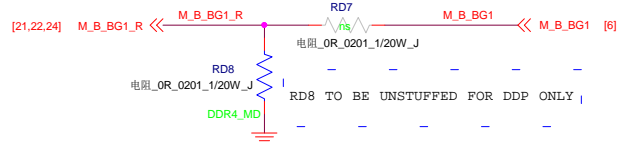
VCCSTG 1x1uf



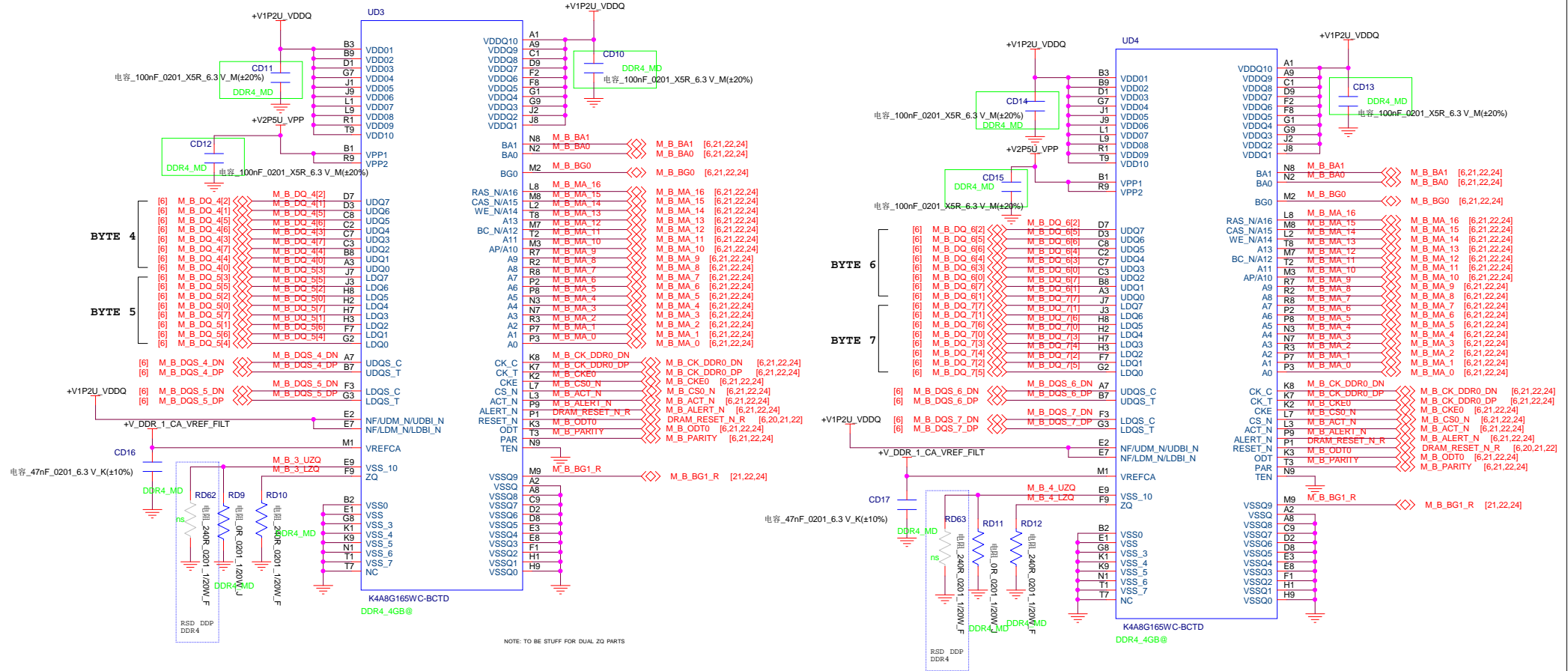
VCCST 1x1uf



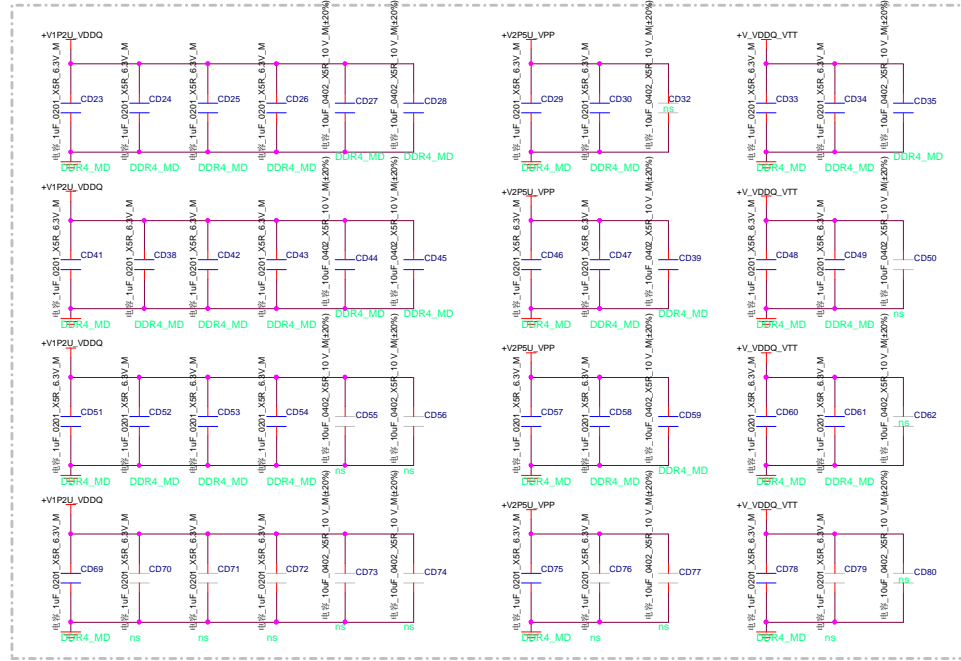
4X1UF
9X10UF
1x22UF



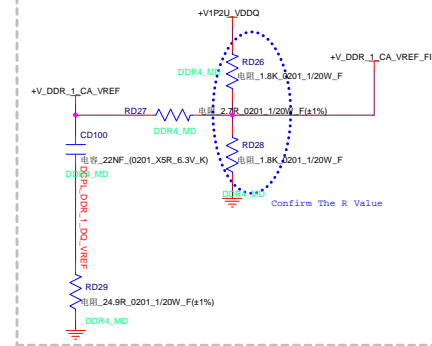
DDR PINS		SDP	DDP
E9	UZQ	GND	240E PD
M9	BG1	GND	BG1 SIG FROM CONTROLLER



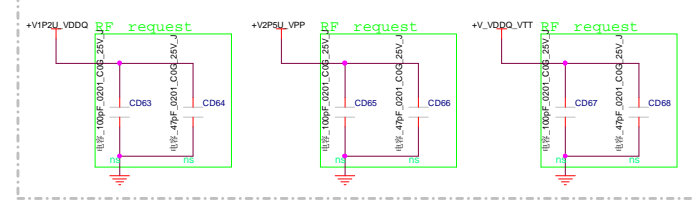
DECOUPLING CAPACITORS FOR DDR CHANNEL B MD



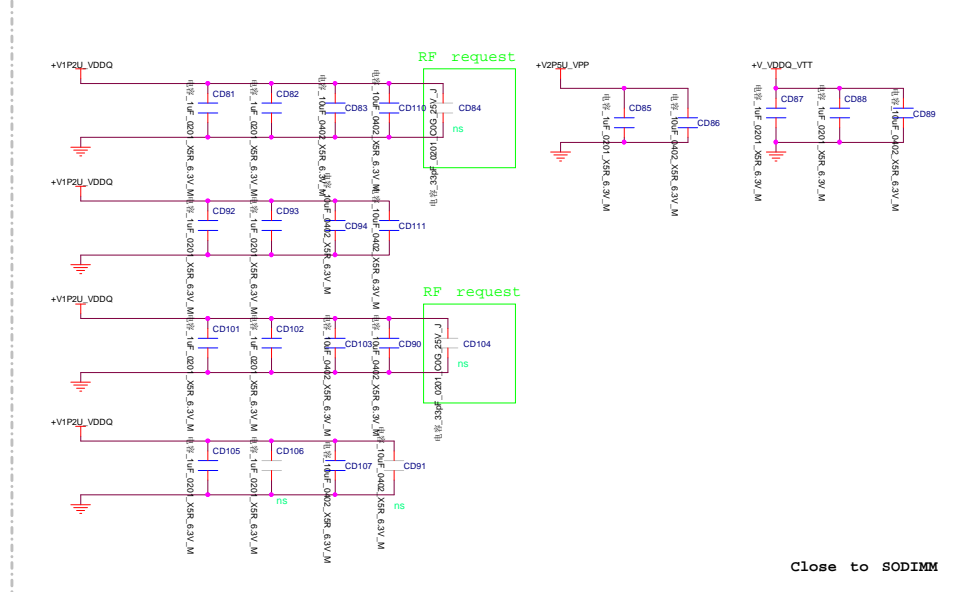
DDR4 CH B MD REF GENERATION



CHB MD

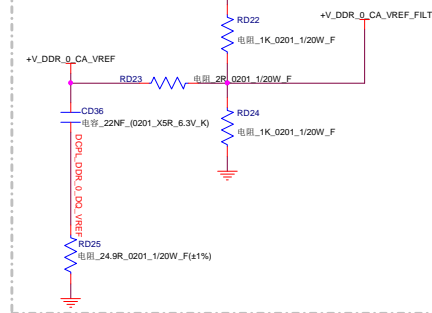


DECOUPLING CAPACITORS FOR DDR CHANNEL A SODIMM



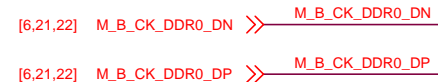
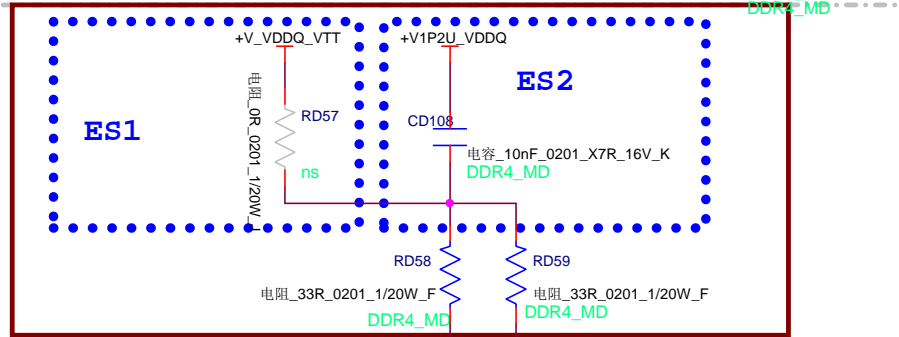
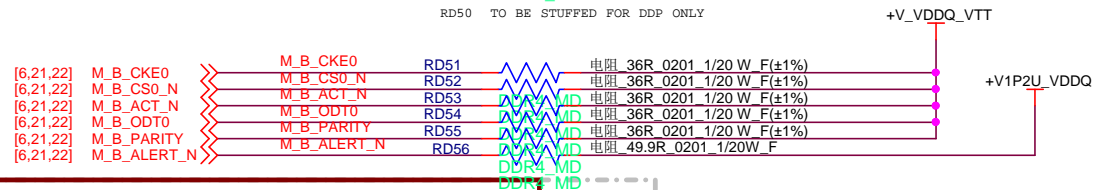
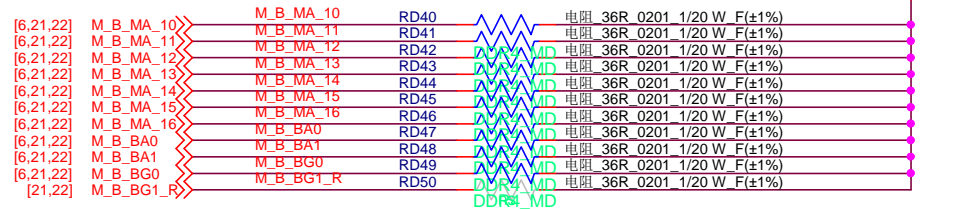
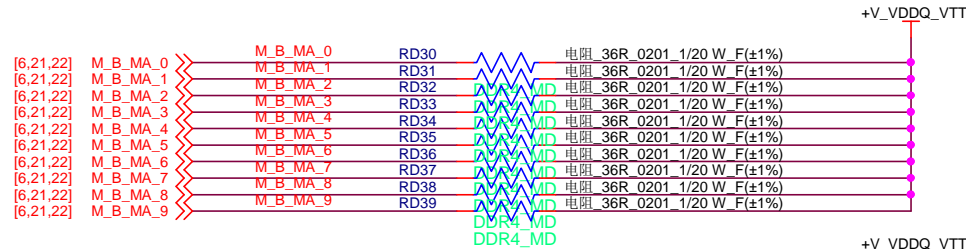
Close to SODIMM

DDR4 CH A SODIMM REF GENERATION



MEMORY TERMINATIONS

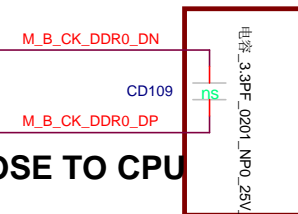
CHANNEL B MD




PLACE TERMINATION RESISTOR CLOSE TO LAST CHIP

- 1.change +V_VDDQ_VTT to +V1P2U_VDDQ
2. add CAP CD155 for ES2 sample - 01/04
3. add RD89 for ES1 sample -01/23

PLACE CLOSE TO CPU

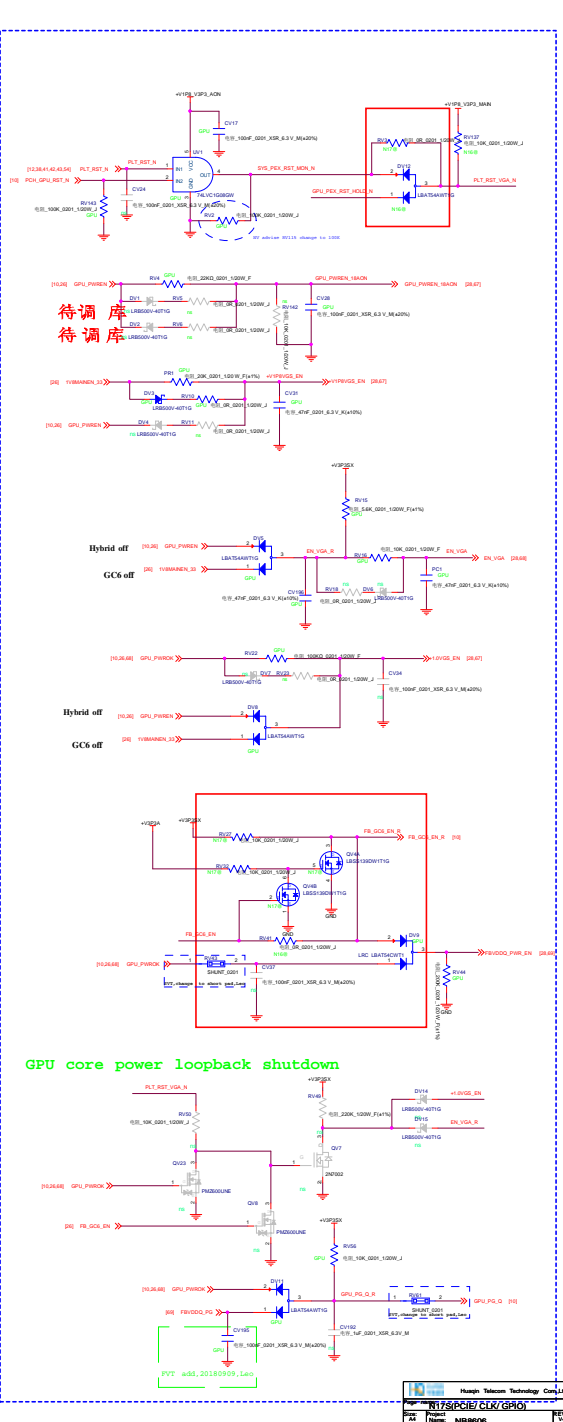
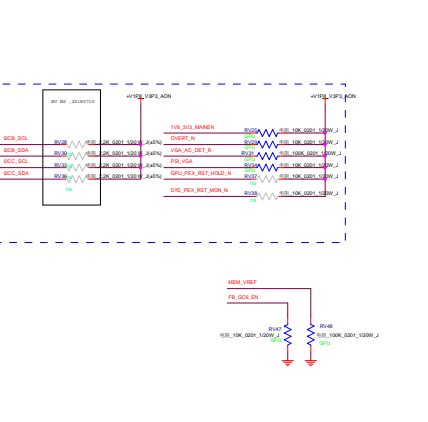
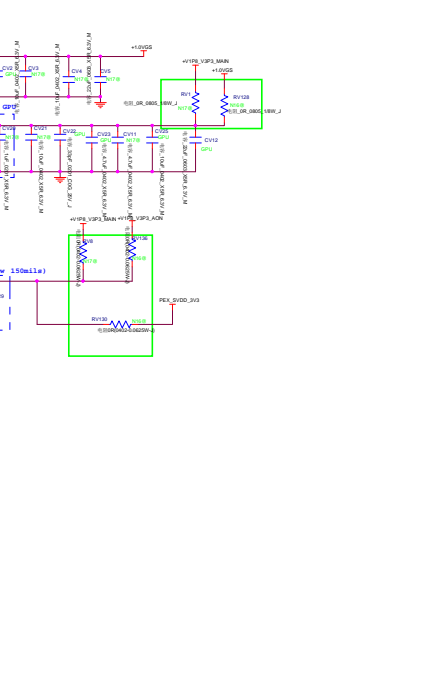
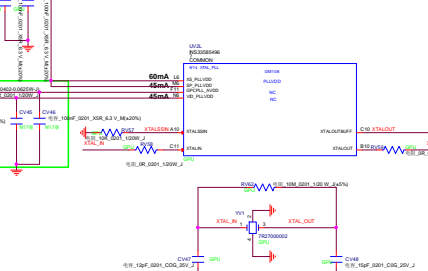
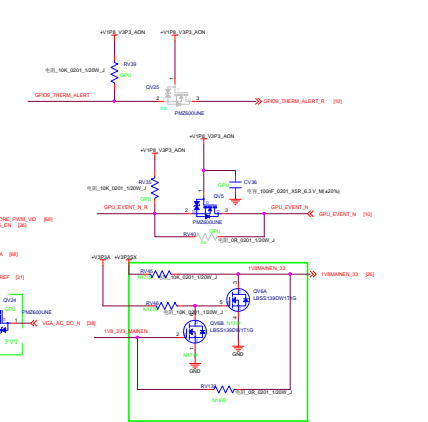
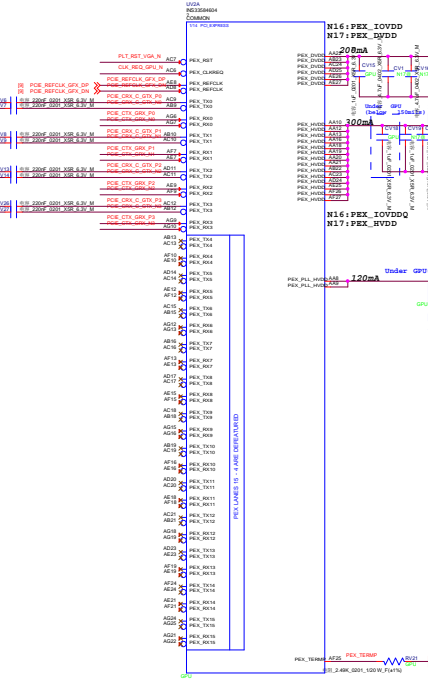
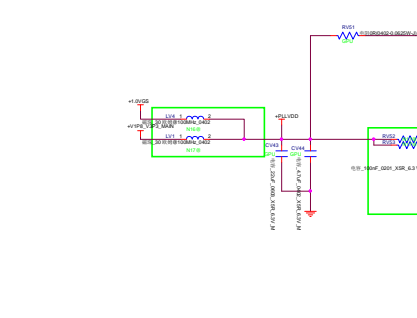
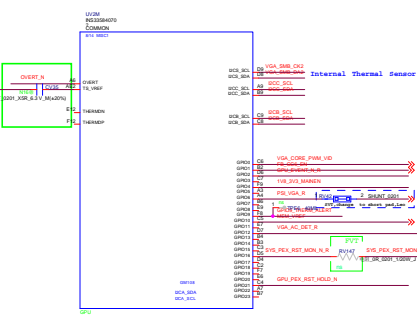
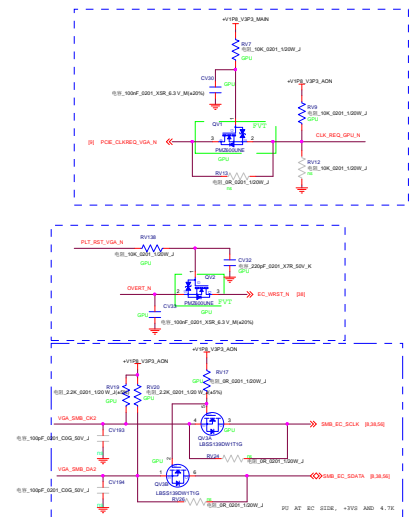


change CD146 to 3.3pF - 01/04

		Huaqin Telecom Technology Co., Ltd.	
Page name: BLANK			
Size: A4	Project Name: NB8606	REV: V4.0	
Date: Thursday, July 18, 2019	Sheet: 25 of 72		

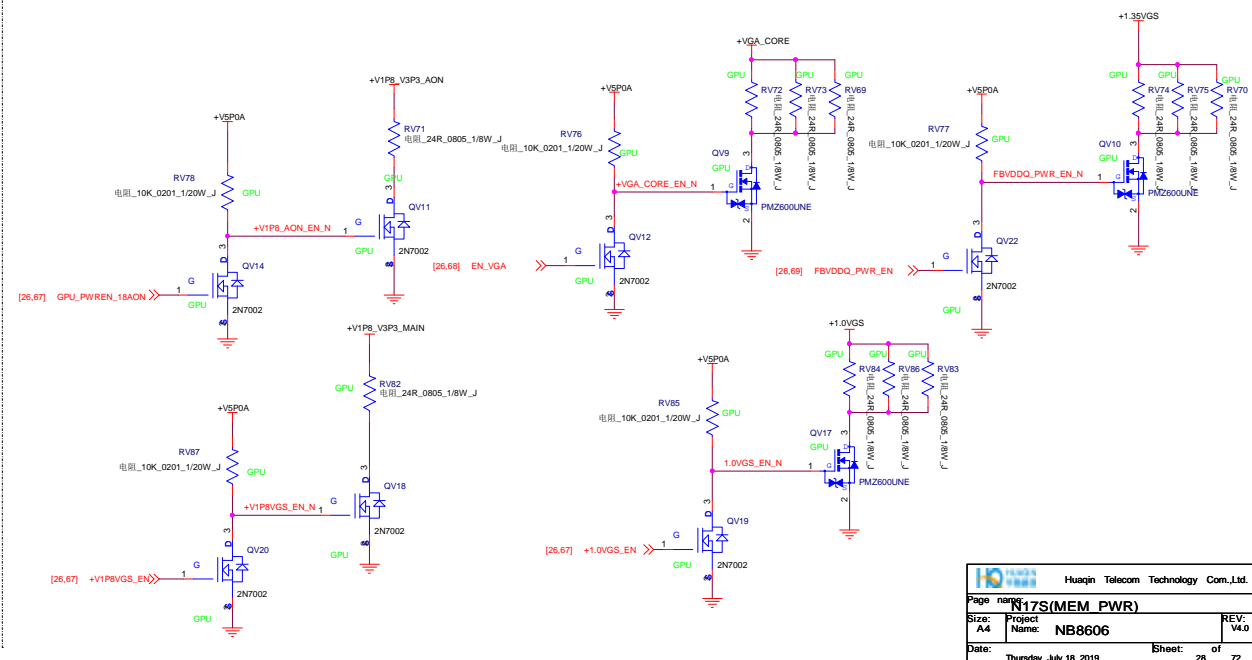
[1] P0E_C0N_C0N_N0-B
[1] P0E_C0N_C0N_P0-B
[1] P0E_C0N_C0N_P0-B
[1] P0E_C0N_C0N_P0-B

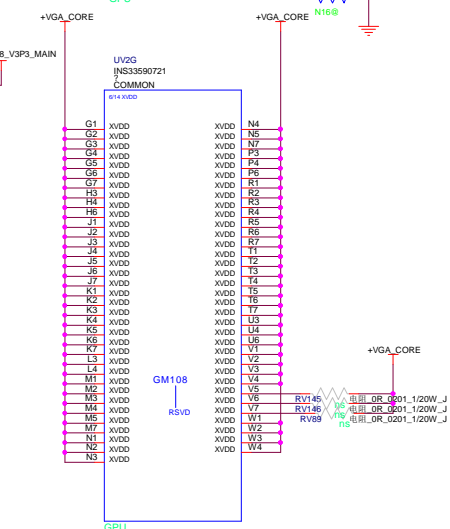
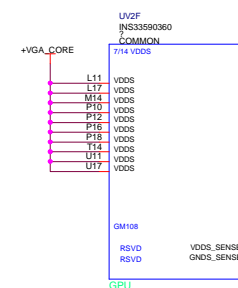
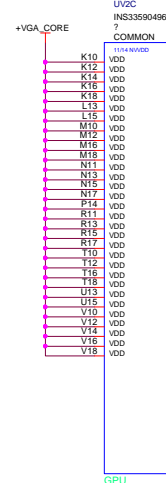
Option
GPU: N16/N17 common part
N16: N16 GPU
N17: N17 GPU



+V1P8A TO +V1P8_AON

Move to Power Page 2018/06/07



[illegible]

For (2018) to (2020)	Rate	Change (2018-2020)	Planned rate (2025)	Planned rate (2035)
FD - 10%	1	1%	1 - 1.1% (2025) 0%	assess[1] 1 - 1.1% (2025) assess[2] 0% (2035) 1 - 1.1% (2035)
FD - 1.1% (2025)	2	1%	1 - 1.1% (2025)	assess[1] 1 - 1.1% (2025) assess[2] 0% (2035) 1 - 1.1% (2035)
FD - 1.1% (2035)	3	1%	1 - 1.1% (2035)	assess[1] 1 - 1.1% (2035) assess[2] 0% (2035) 1 - 1.1% (2035)
FD - 1.1% (2035)	4	1%	1 - 1.1% (2035)	assess[1] 1 - 1.1% (2035) assess[2] 0% (2035) 1 - 1.1% (2035)
FD - 1.1% (2035)	5	1%	1 - 1.1% (2035)	assess[1] 1 - 1.1% (2035) assess[2] 0% (2035) 1 - 1.1% (2035)
FD - 1.1% (2035)	6	1%	1 - 1.1% (2035)	assess[1] 1 - 1.1% (2035) assess[2] 0% (2035) 1 - 1.1% (2035)

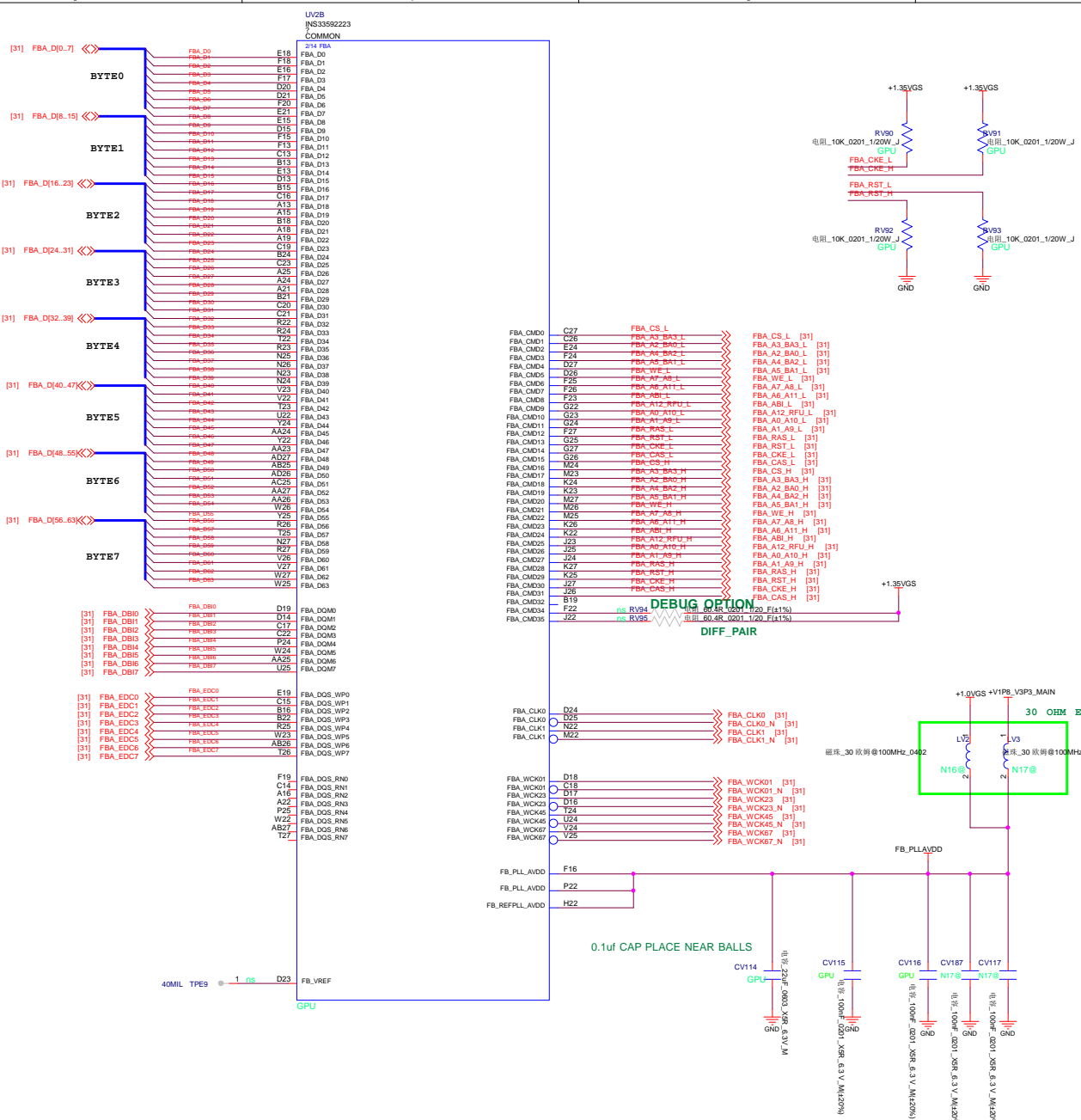



Table 7-4. GDDR5 Mode H Mapping


G82-64, G82B-64, G84B-128	Channel D 0...31	G82-64, G82B-64, G84B-128	Channel I 32...63
CHD0	CS*	CHD16	CS*
CHD1	A3_BA3	CHD17	A3_BA2
CHD2	A2_BA0	CHD18	A2_BA0
CHD3	A4_BA2	CHD19	A4_BA3
CHD4	A5_BA1	CHD20	A5_BA1
CHD5	WE*	CHD21	WE*
CHD6	A7_A8	CHD22	A7_A8
CHD7	A6_A11	CHD23	A6_A11
CHD8	AB*	CHD24	AB*
CHD9	A12_RFU	CHD25	A12_RFU
CHD10	A0_A10	CHD26	A0_A10
CHD11	A1_A9	CHD27	A1_A9
CHD12	RA5*	CHD28	RA5*
CHD13	RS1*	CHD29	RS1*
CHD14	CR2*	CHD30	CR2*
CHD15	CAS*	CHD31	CAS*
G82-64, G82B-64, G84B-128 Channel H 0...31			
CHD32	Hot used		
CHD33	Hot used		
CHD34	DEBUG0		
CHD35	DEBUG1		

Notes:
 1. Not available in G82B-64 and G84B-128 packages.
 2. GPU debug pins not connected to G82B-64. See section 7.1.13.


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		Huaqin Telecom Technology Co., Ltd.	
Page name: BLANK			
Size: A4	Project Name: NB8606	REV: V4.0	
Date: Thursday, July 18, 2019	Sheet: 33		of 72


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

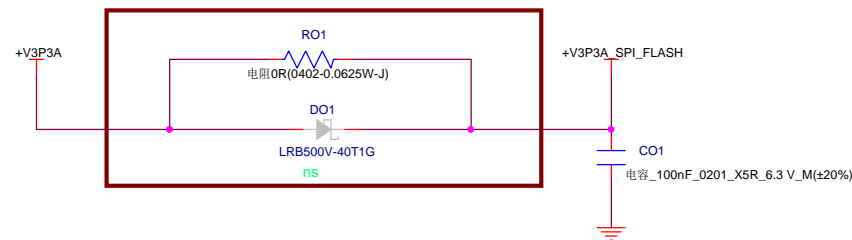
		Huaqin Telecom Technology Com.,Ltd.	
Page name: BLANK			
Size: A4	Project Name: NB8606		REV: V4.0
Date: Thursday, July 18, 2019	Sheet: 34		of 72

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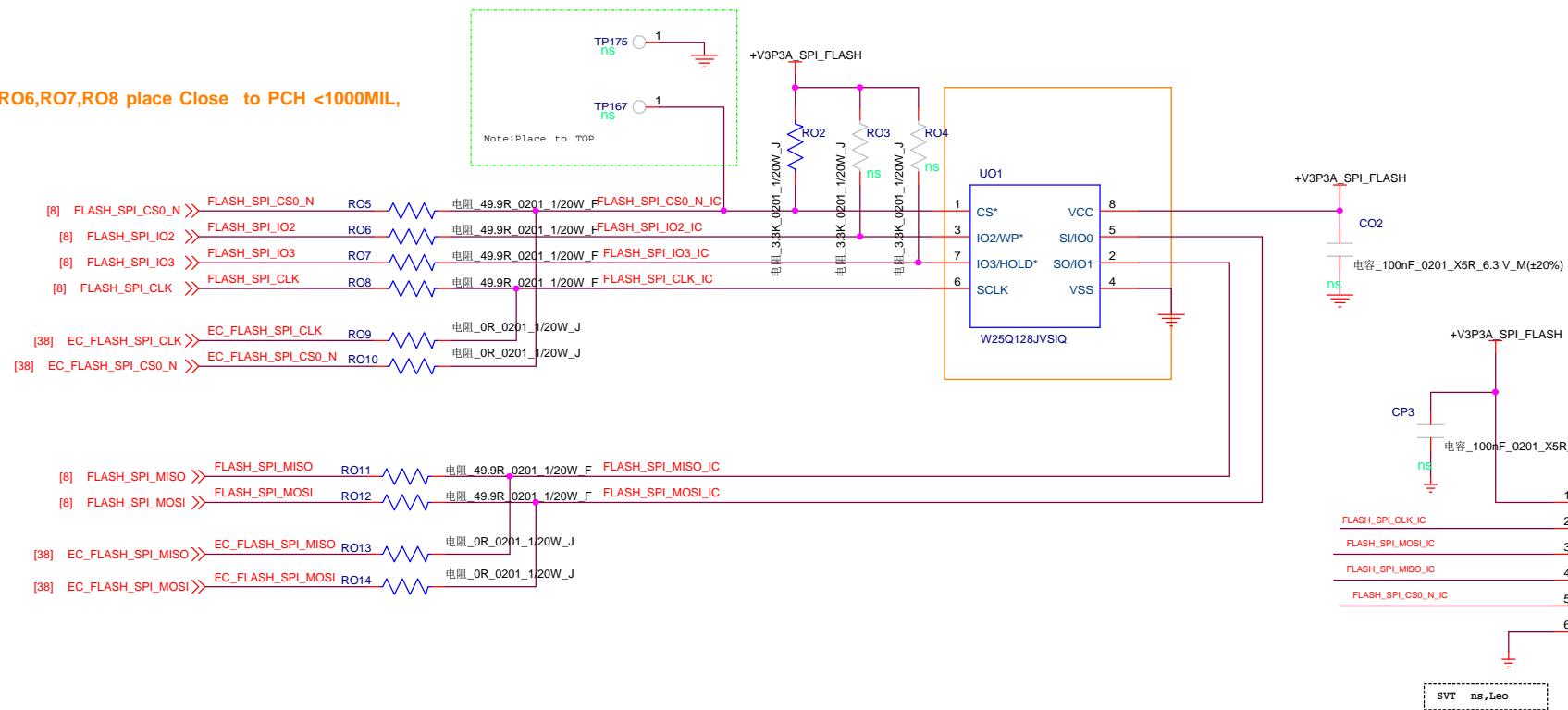
		Huaqin Telecom Technology Com.,Ltd.	
Page name: BLANK			
Size: A4	Project Name: NB8606		REV: V4.0
Date: Thursday, July 18, 2019	Sheet: 35 of 72		

5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				

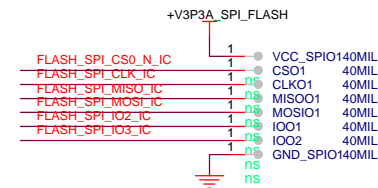
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Size: A4	Project Name: NB8606		REV: V4.0
Date: Thursday, July 18, 2019	Sheet: 36 of 72		



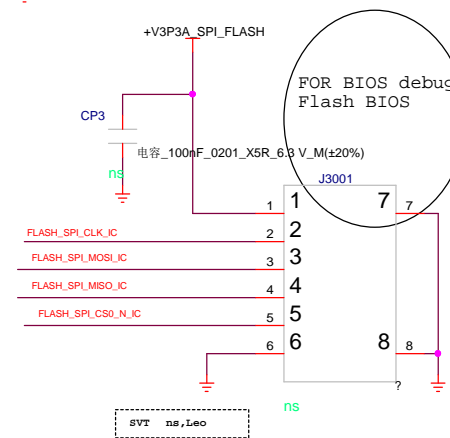
Series RO5,RO6,RO7,RO8 place Close to PCH <1000MIL,

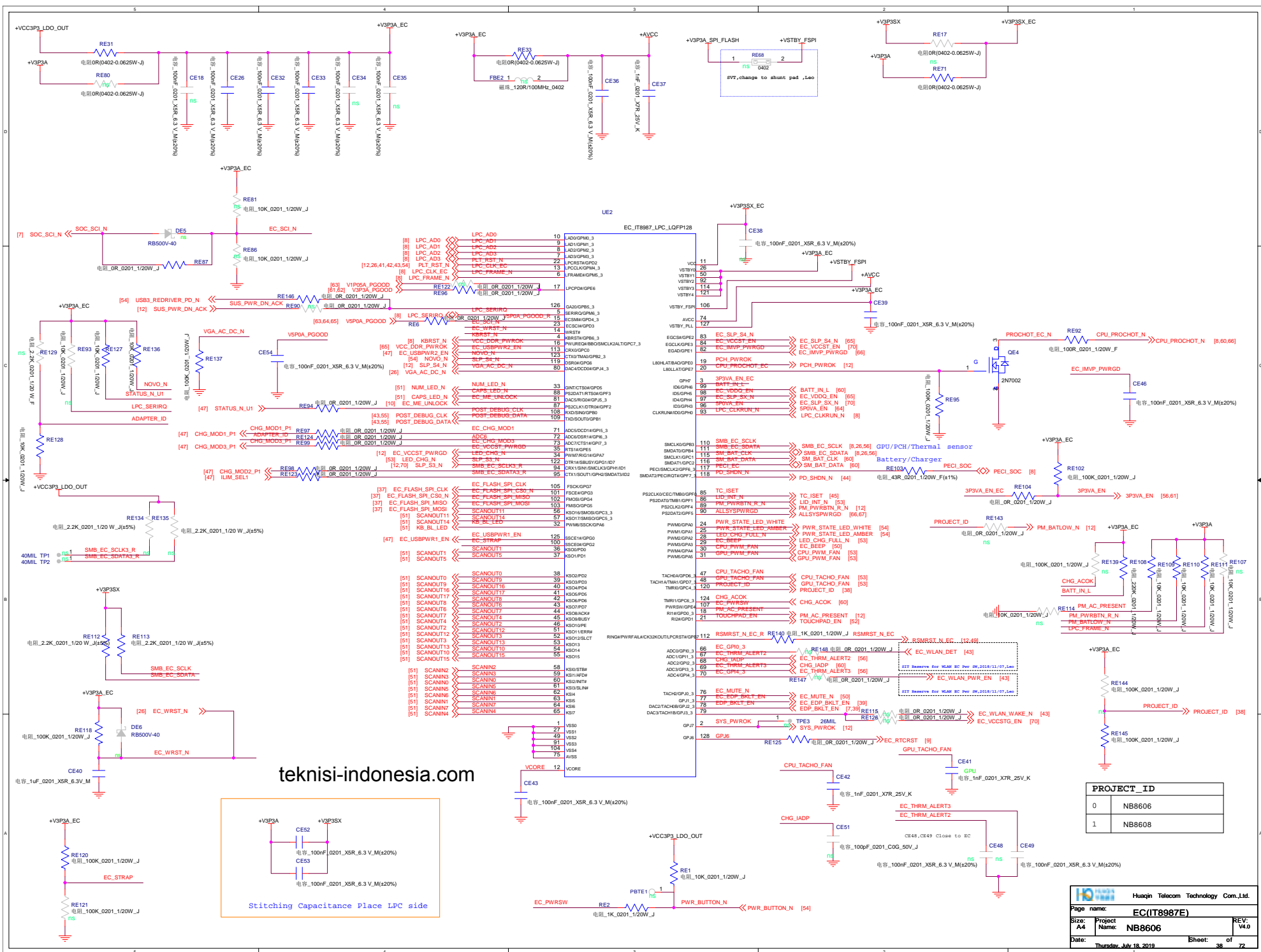


FOR product line

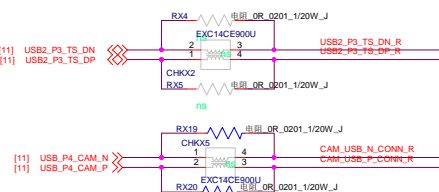
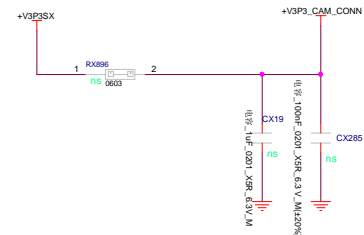
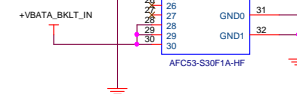
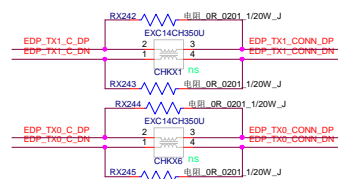


FOR BIOS debug
Flash BIOS

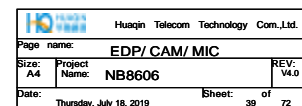
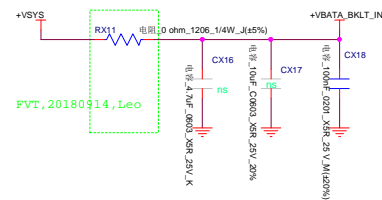
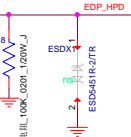
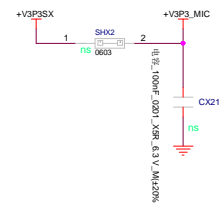




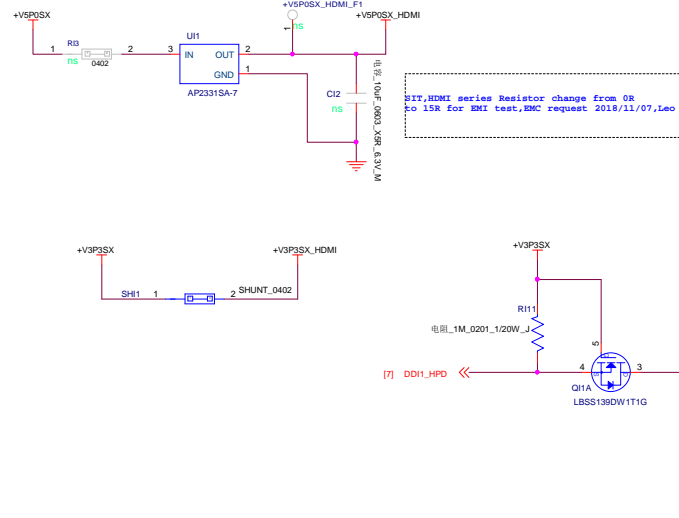
eDP & CAM & MIC CONN



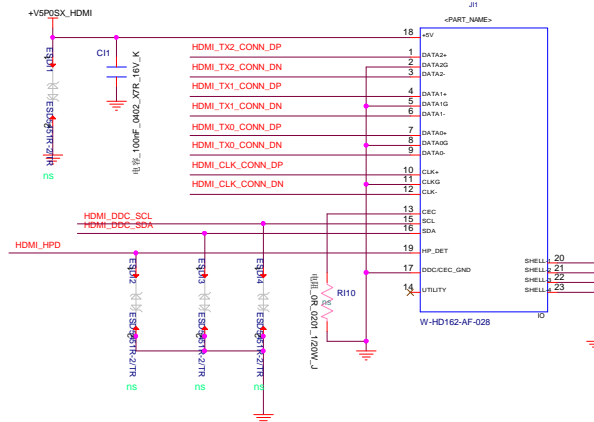
SVT,DEL +V3P3_TS 2019/01/02 ,Leo



Power 1



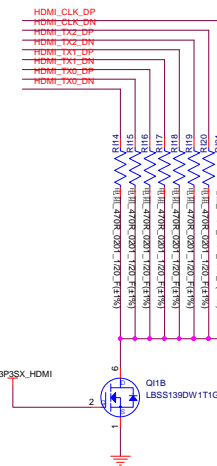
HDMI CONN



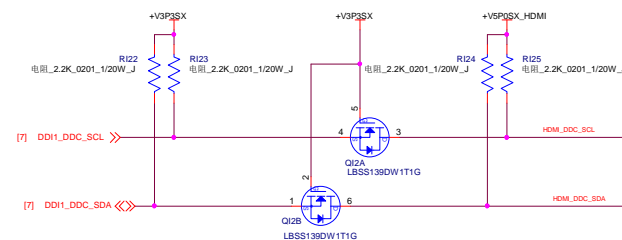
Signal

HDMI_CLK_DP	C13	电容 100nF 0201 X5R 10V K	DDI1_TX3_DP	DDI1_TX3_DP	[7]
HDMI_CLK_DN	C14	电容 100nF 0201 X5R 10V K	DDI1_TX3_DN	DDI1_TX3_DN	[7]
HDMI_TX0_DP	C15	电容 100nF 0201 X5R 10V K	DDI1_TX2_DP	DDI1_TX2_DP	[7]
HDMI_TX0_DN	C16	电容 100nF 0201 X5R 10V K	DDI1_TX2_DN	DDI1_TX2_DN	[7]
HDMI_TX1_DP	C17	电容 100nF 0201 X5R 10V K	DDI1_TX1_DP	DDI1_TX1_DP	[7]
HDMI_TX1_DN	C18	电容 100nF 0201 X5R 10V K	DDI1_TX1_DN	DDI1_TX1_DN	[7]
HDMI_TX2_DP	C19	电容 100nF 0201 X5R 10V K	DDI1_TX0_DP	DDI1_TX0_DP	[7]
HDMI_TX2_DN	C110	电容 100nF 0201 X5R 10V K	DDI1_TX0_DN	DDI1_TX0_DN	[7]

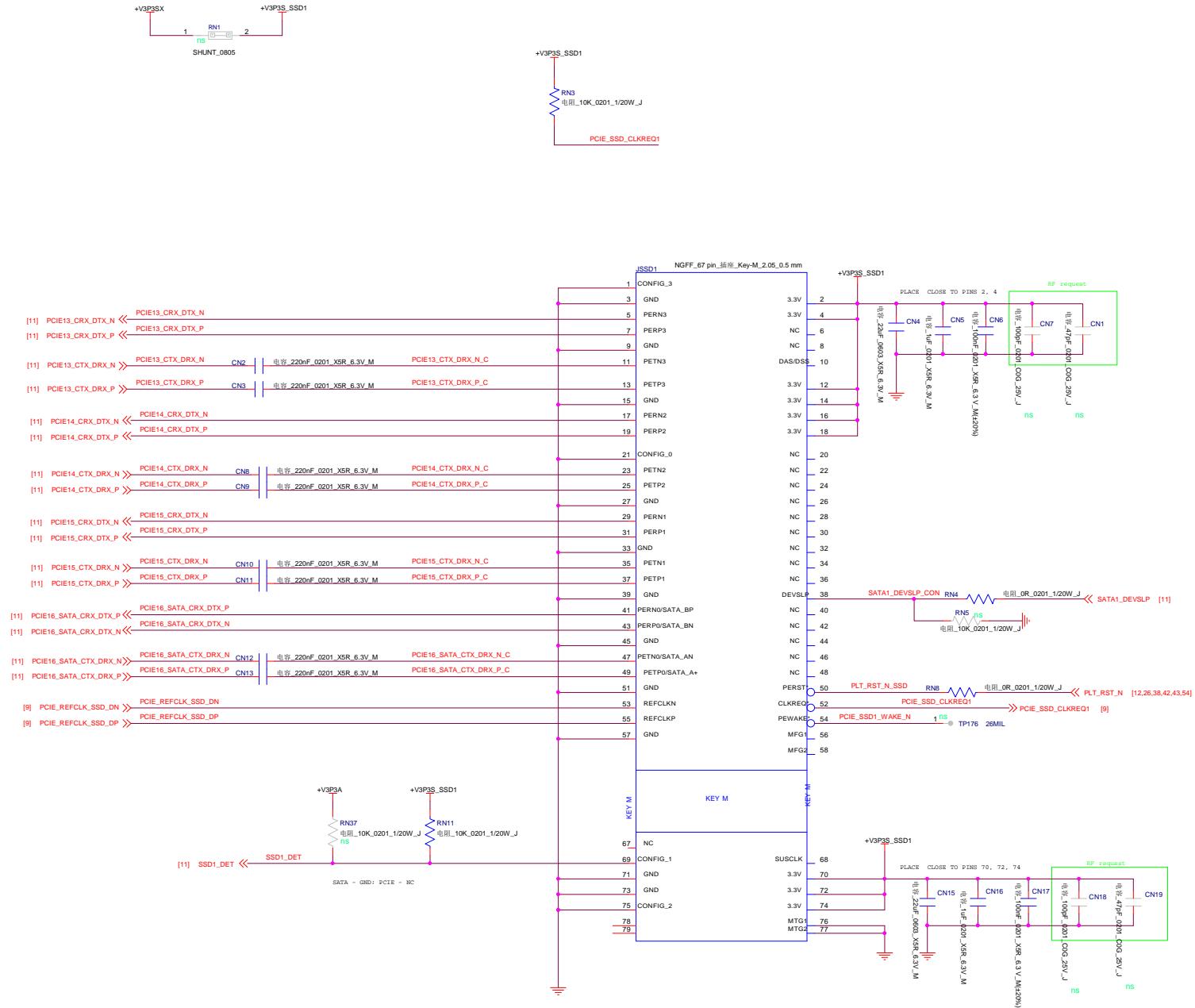
WHL---HDMI 1.4b level shift



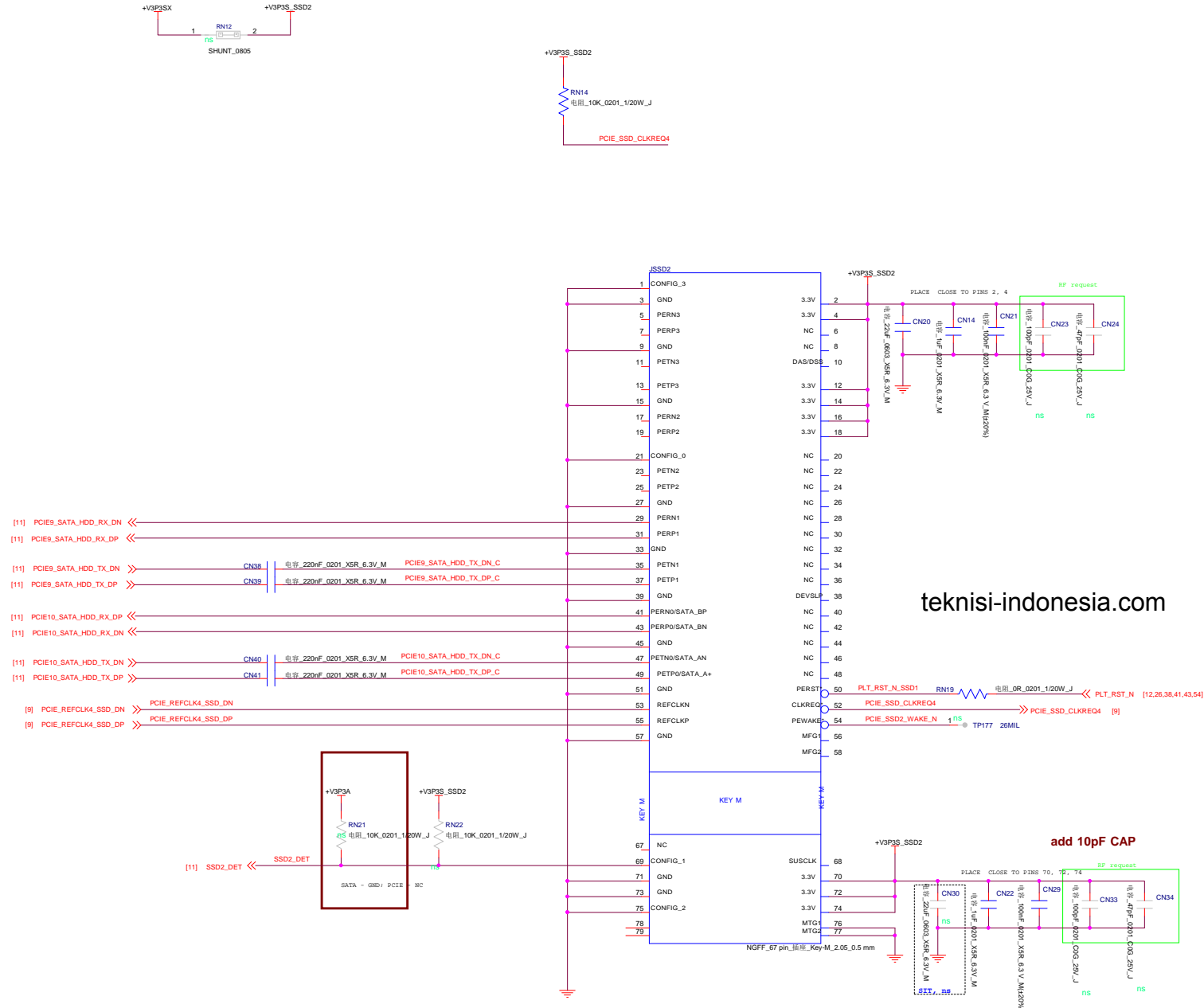
ESD

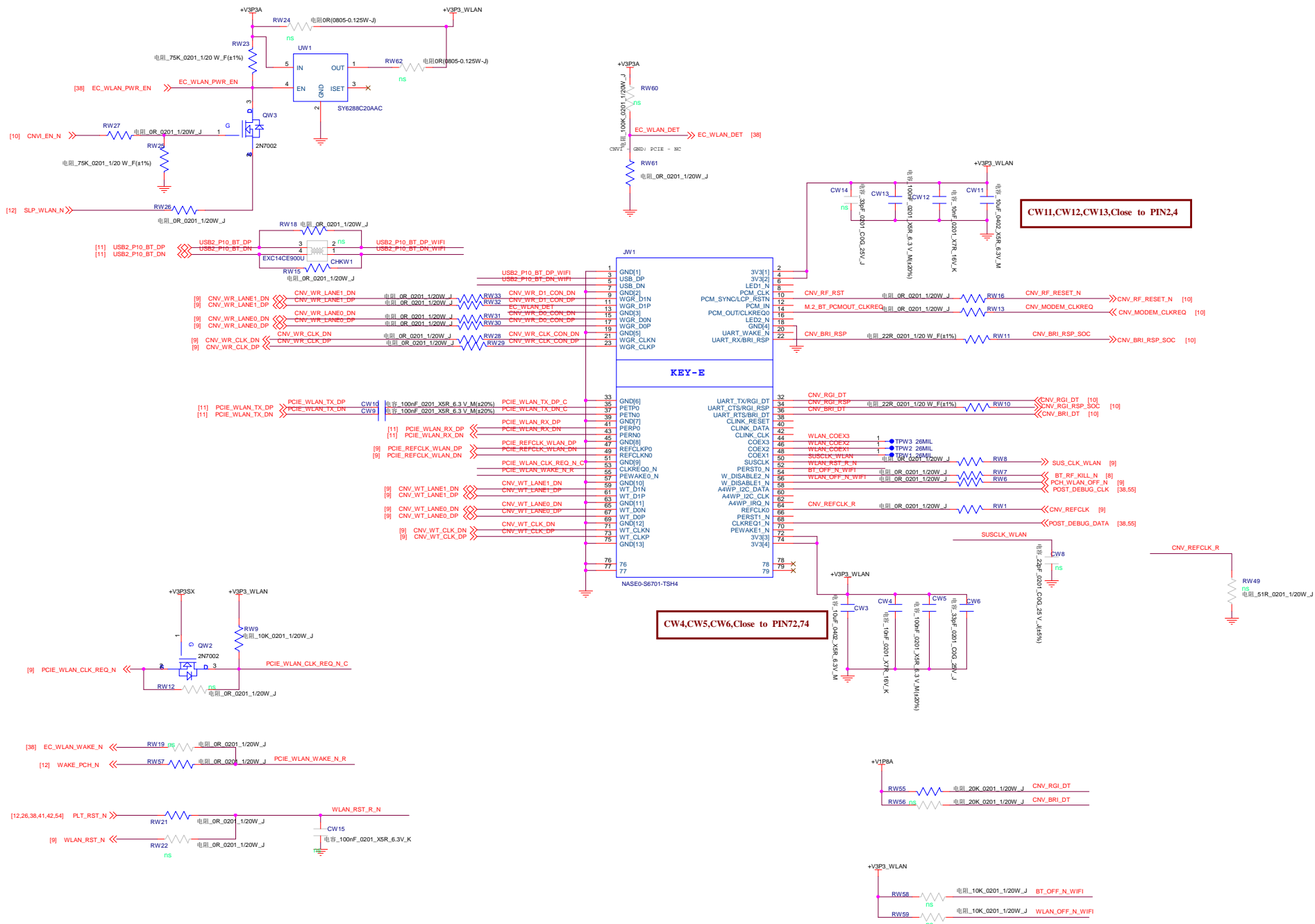


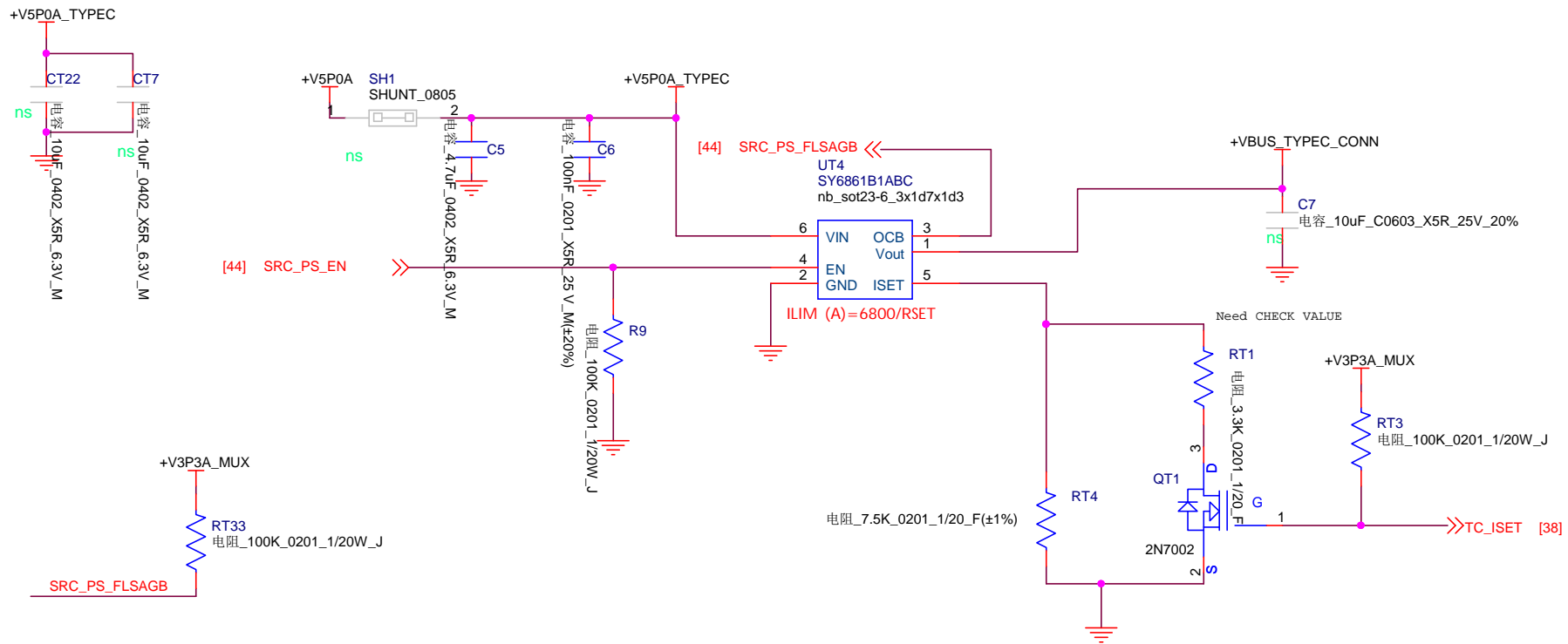
SSD



SSD 2

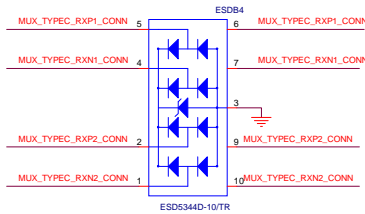
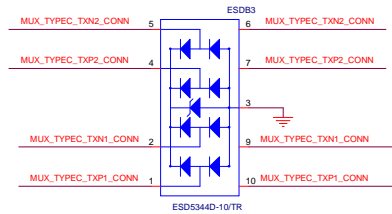




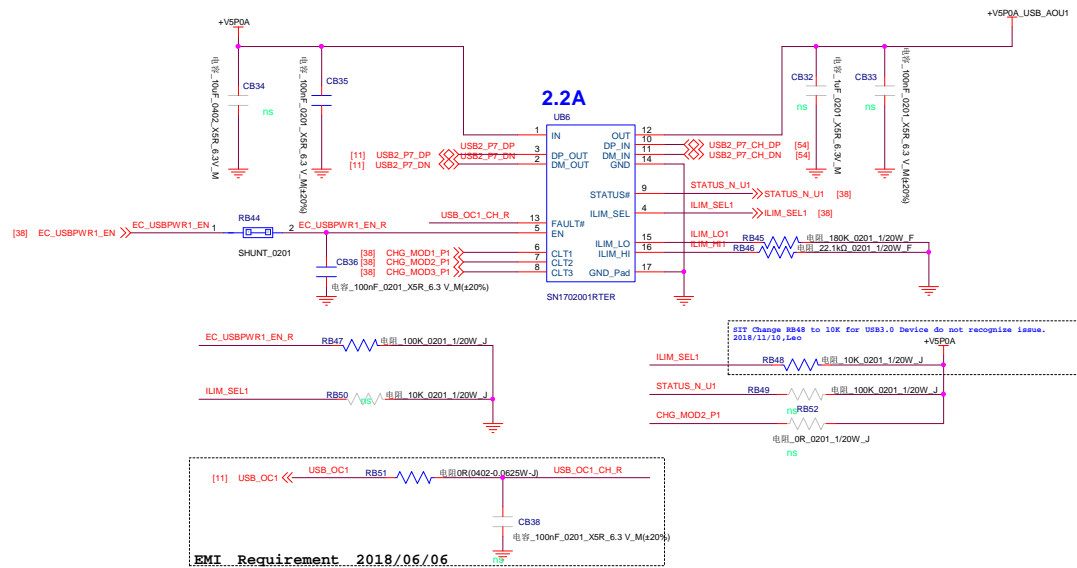


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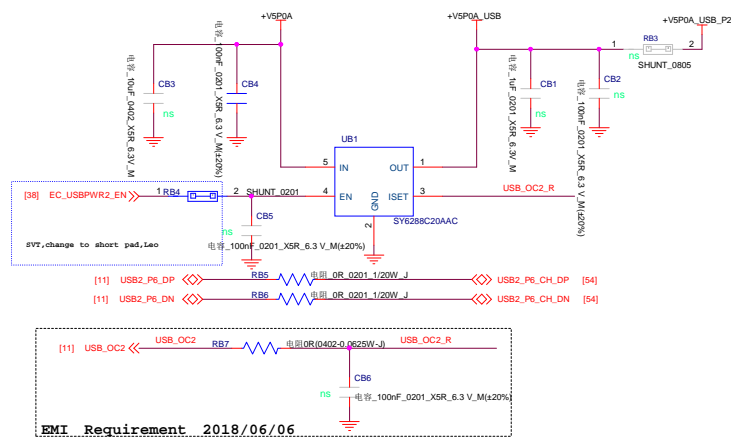
TYPE-C_ESD



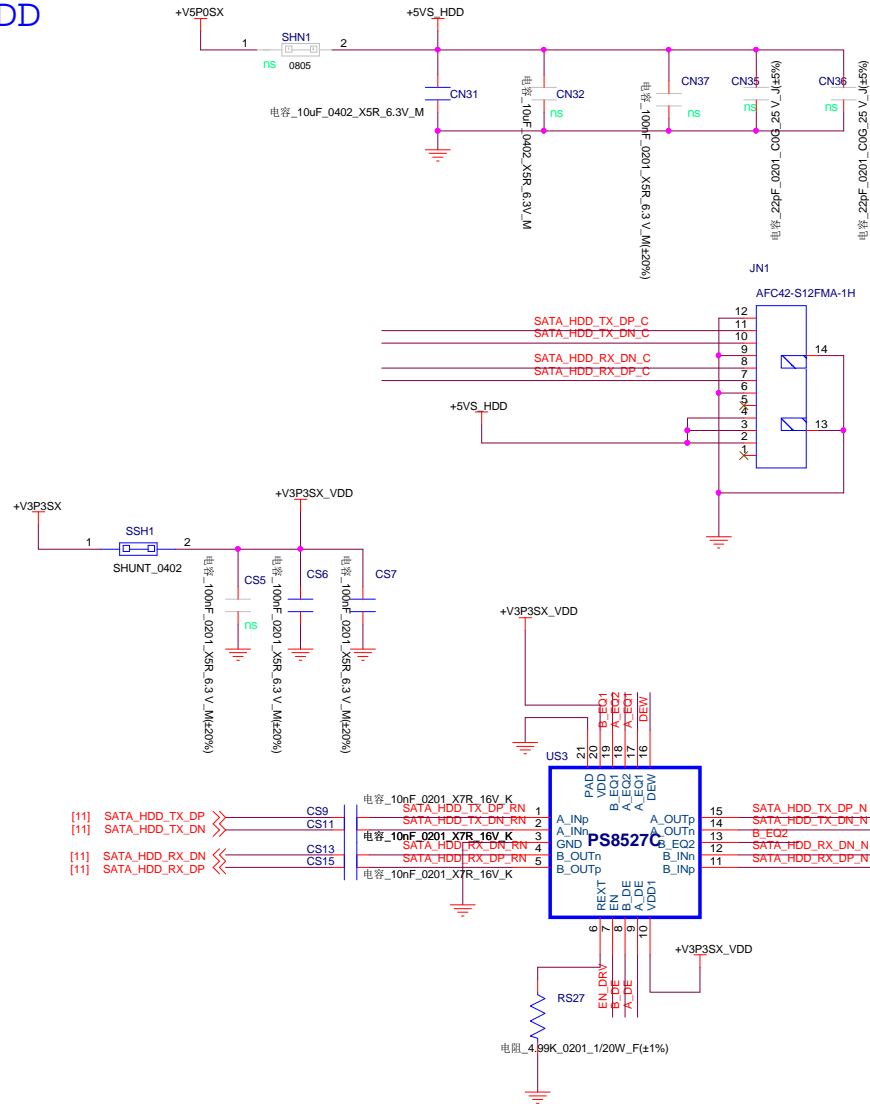
USB3.1 POWER Port1



USB3.1 POWER Port2



HDD



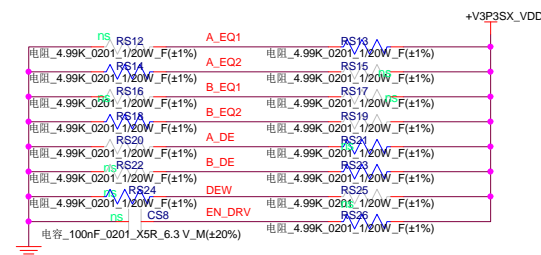
A_EQ:14.4db;B_EQ:2.4db
FVT

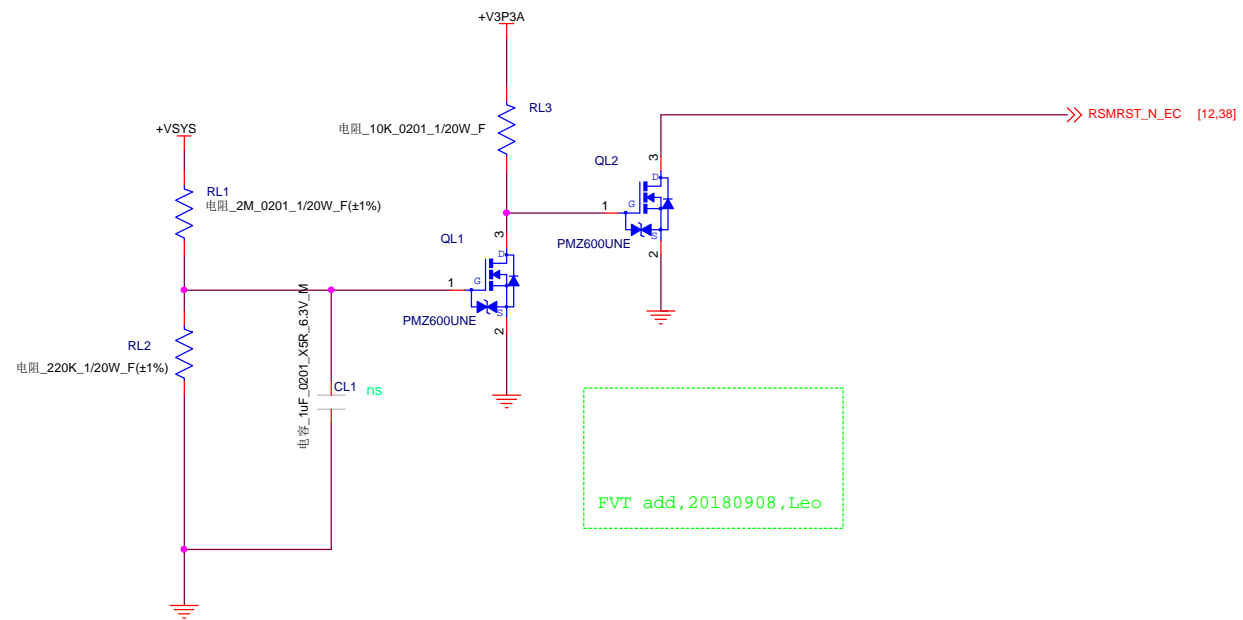
PS8527C


Equalization level setting for Channel x(x=A/B), internally tied to VDD/2
[x_EQ2, x_EQ1] ==
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

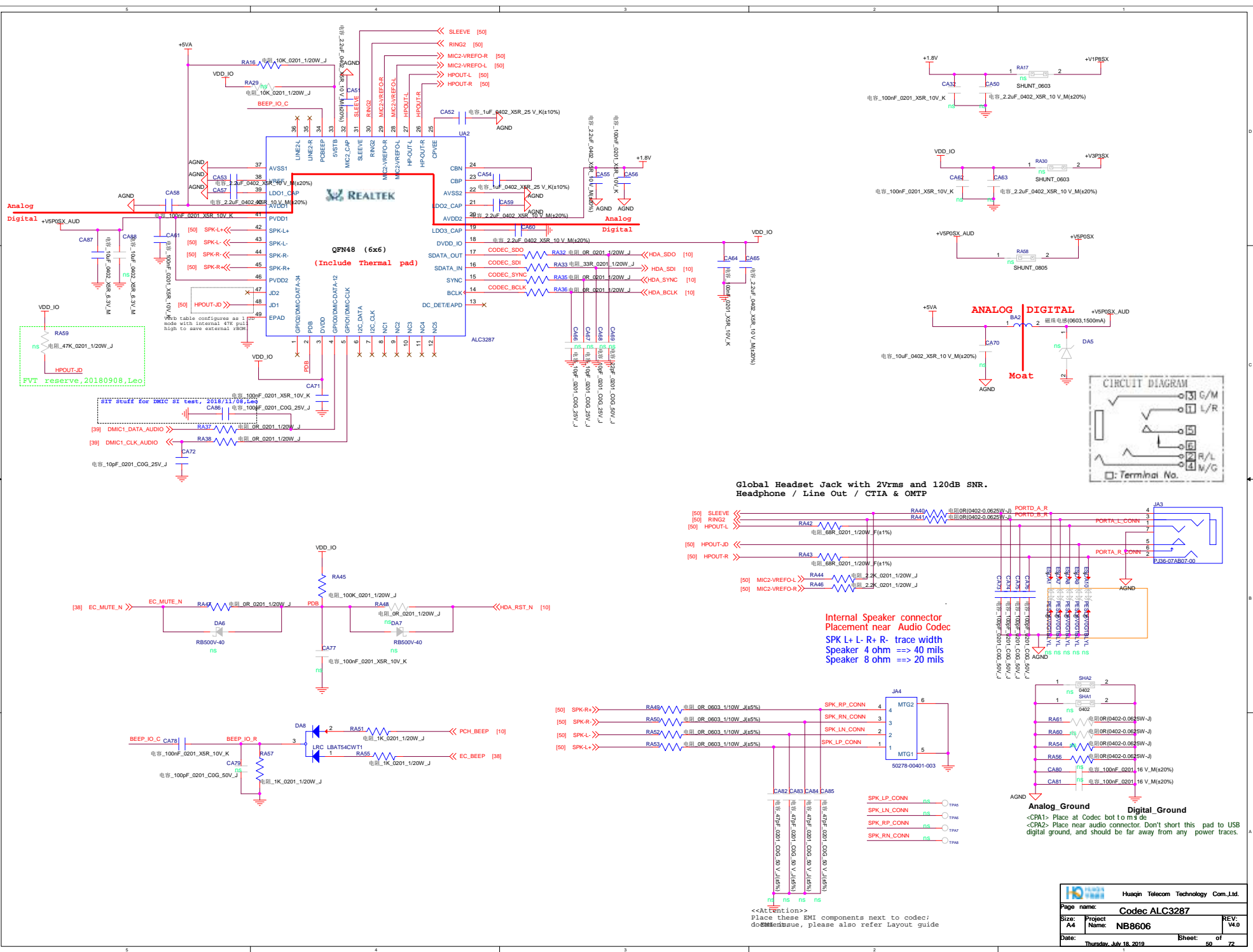
De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2
[x_DE] ==
M: -3.5dB
L: 0dB
H: -6dB

De-emphasis width adjustment, internally pulled down
[DEW] ==
L: for SATA3
H: for SATA2

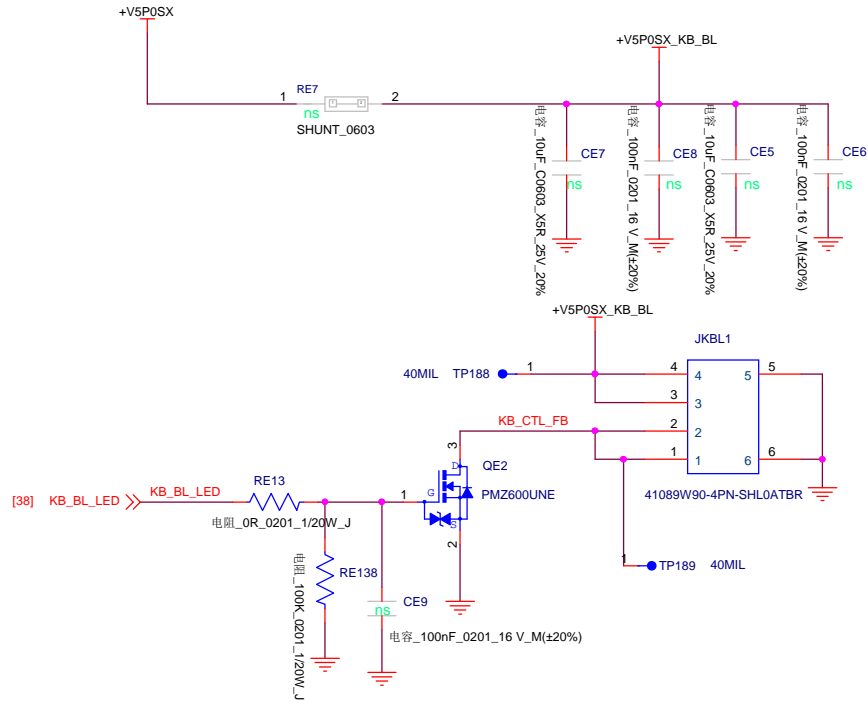




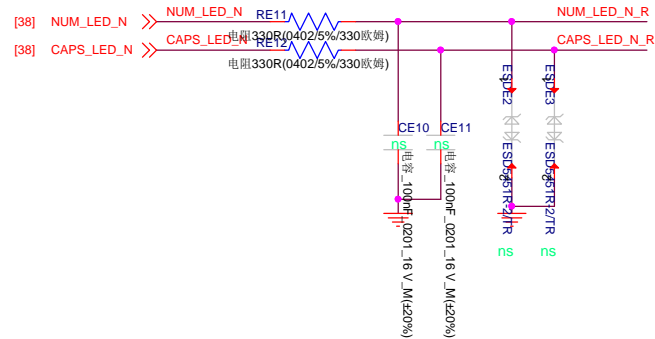
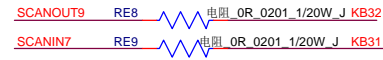
		Huaqin Telecom Technology Com.,Ltd.	
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Size: A4	Project Name: NB8606	REV: V4.0	
Date: Thursday, July 18, 2019	Sheet: 49		of 72



KB Backlight



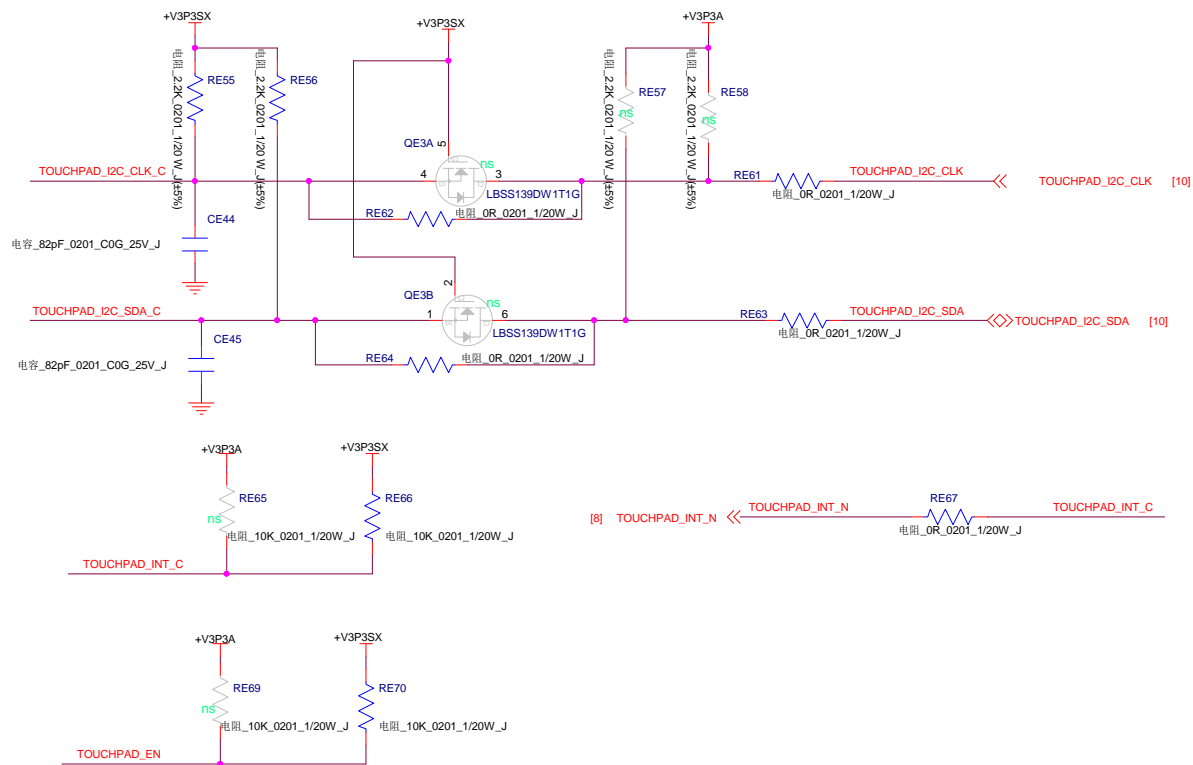
KB CONN



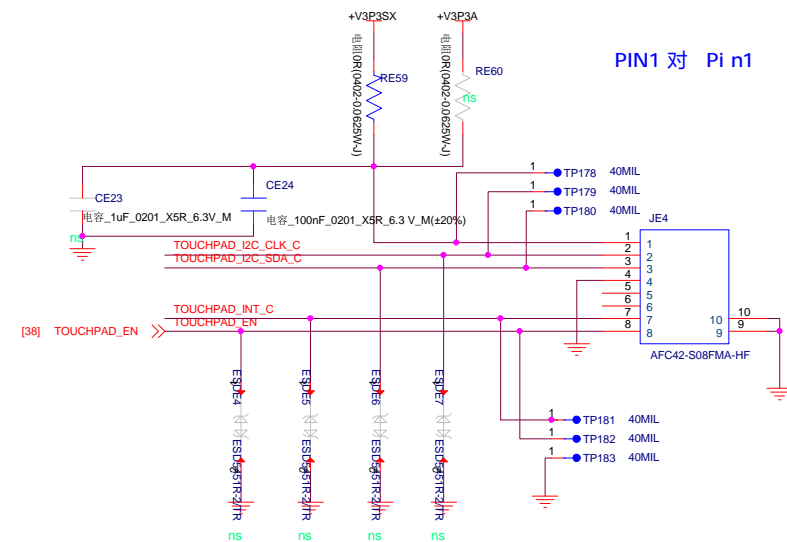
+V3P3SX

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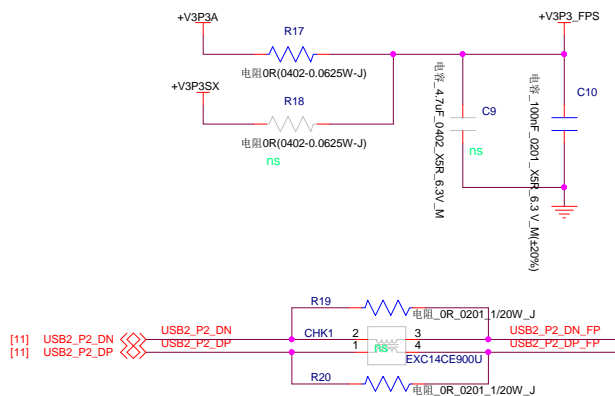
Touch Pad



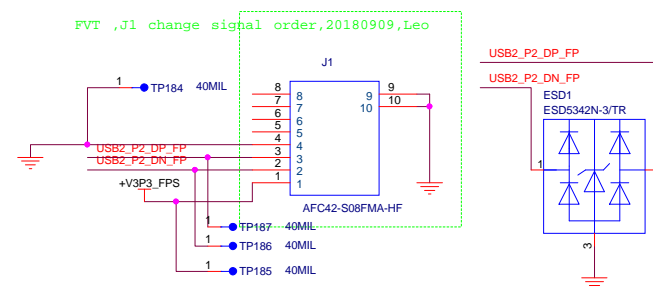
Touch Pad CONN



Finger Print

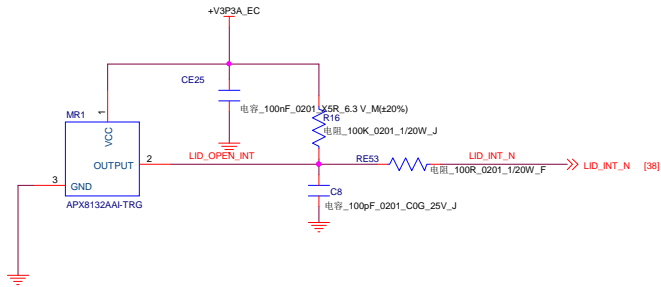


Finger Print CONN



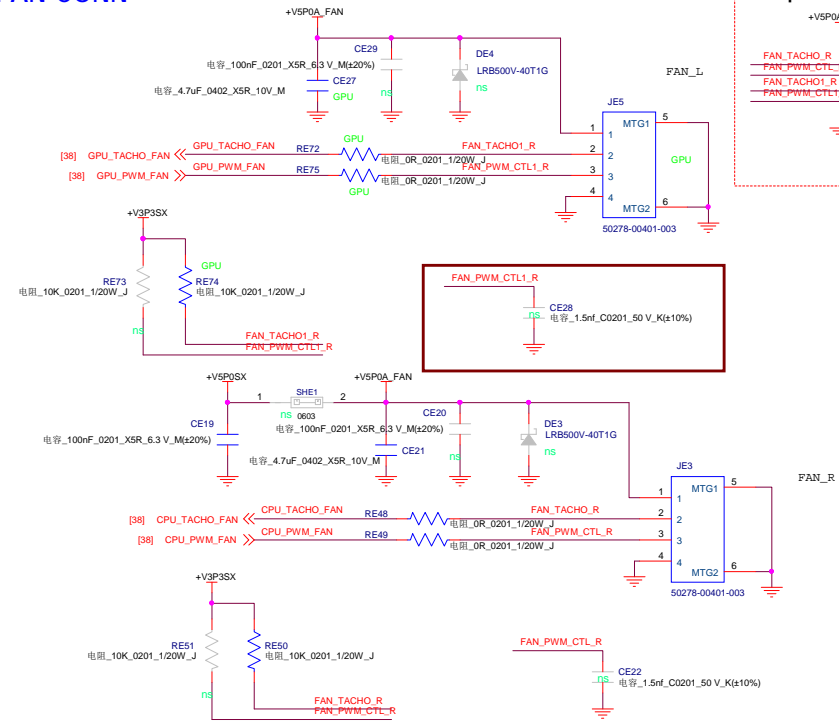
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Page name: TouchPad/ Finger Print			
Size: A4	Project Name: NB8606	REV: V4.0	
Date: Thursday, July 18, 2019	Sheet: 52	of 72	

PWR BUTTON LOGIC

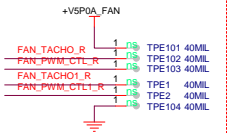


HALL

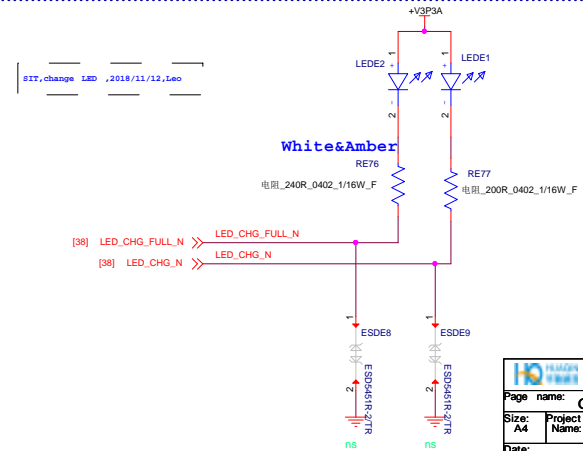
FAN CONN

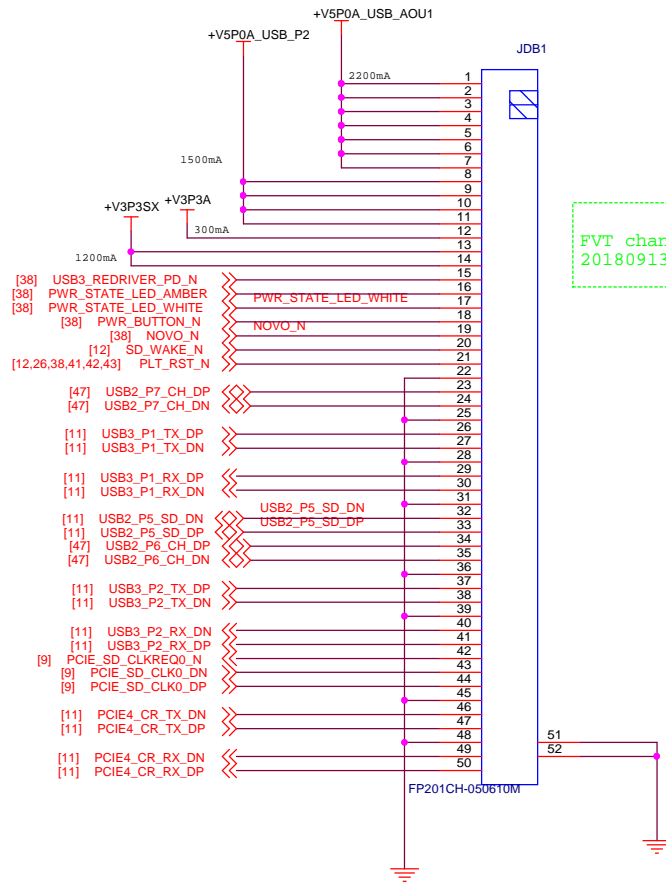


FOR product line

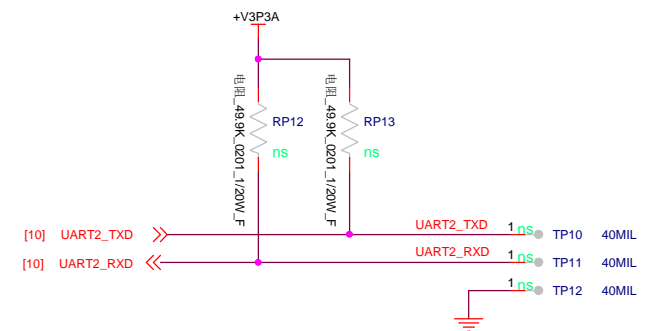


LED



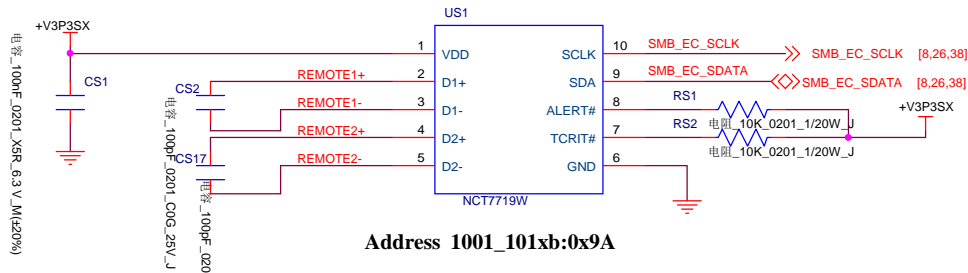


FVT change to 50pin for USB Drop test,
20180913

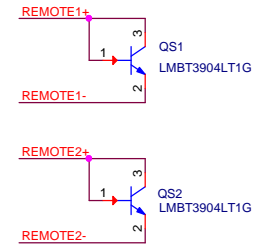


REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"
Connect guard traces to GND on either side of the
DXP-DXN traces

Close to charger

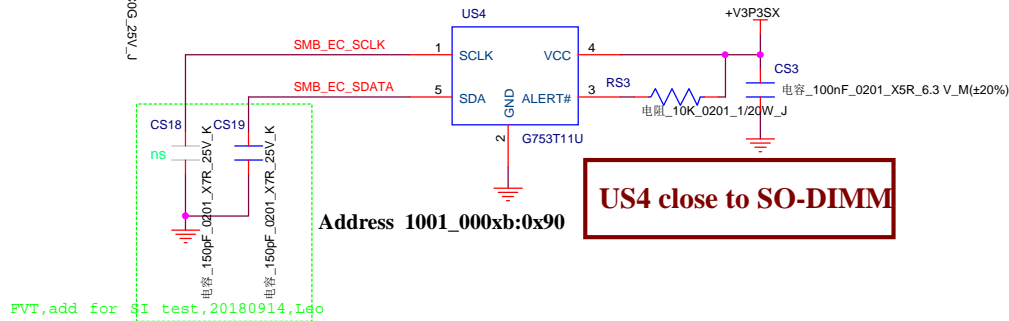


Between CPU and GPU

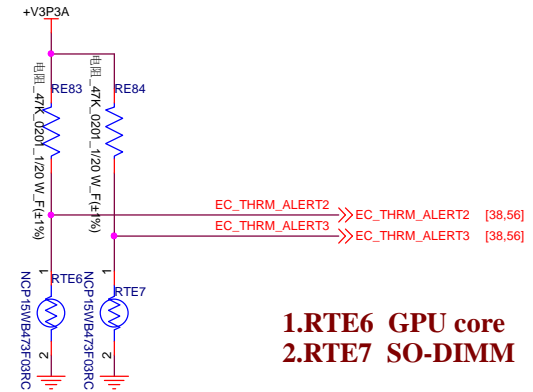


Address 1001_000xb:0x90

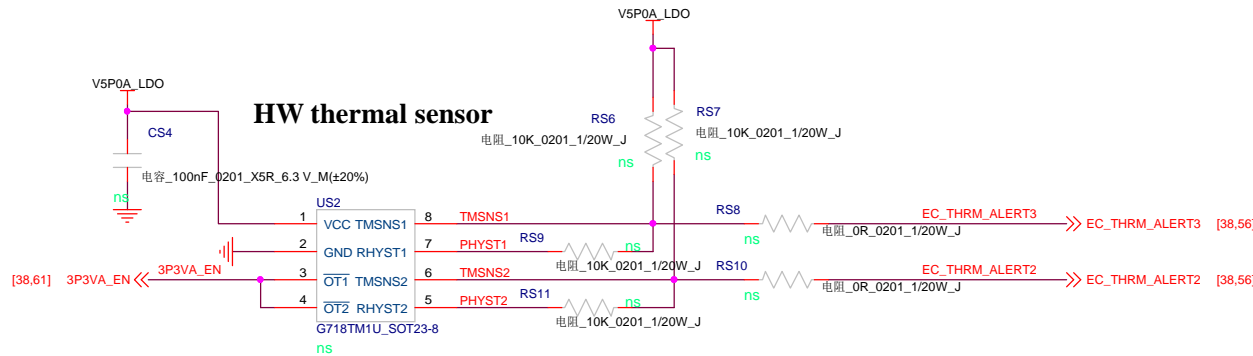
US4 close to SO-DIMM



1.RTE6 GPU core
2.RTE7 SO-DIMM



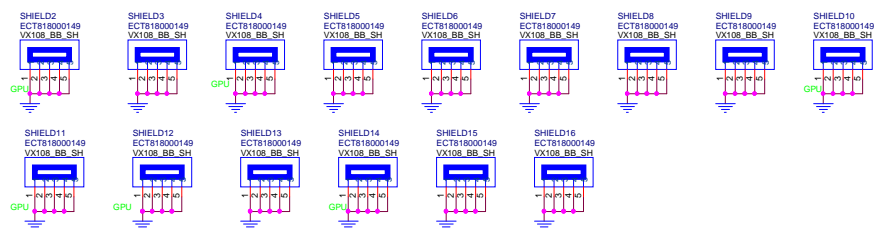
HW thermal sensor



NOTE:
HW thermal sensor??

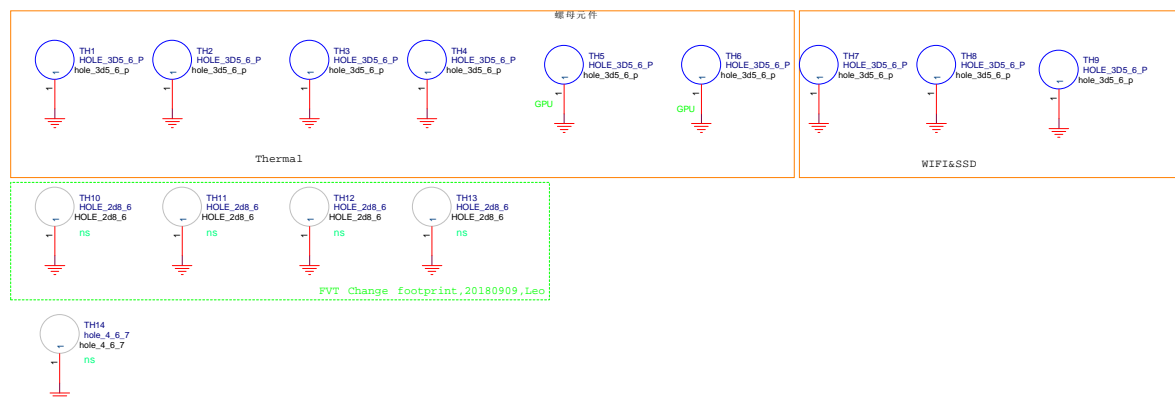
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

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Page name:	Thermal sensor
Size: A4	Project Name: NB8606
Date: Thursday, July 18, 2019	REV: V4.0
Sheet: 56	of 72



屏蔽 罩夹 子*15

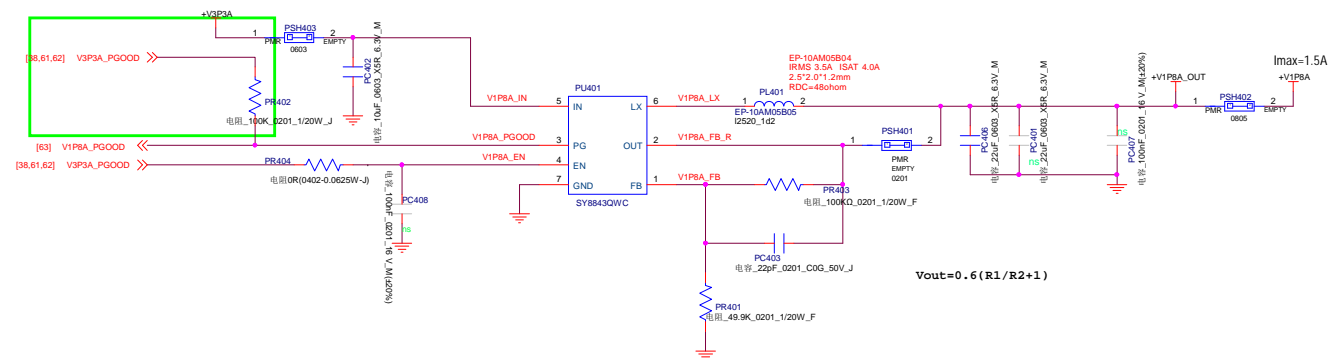
Need add HQ CODE and Stuff

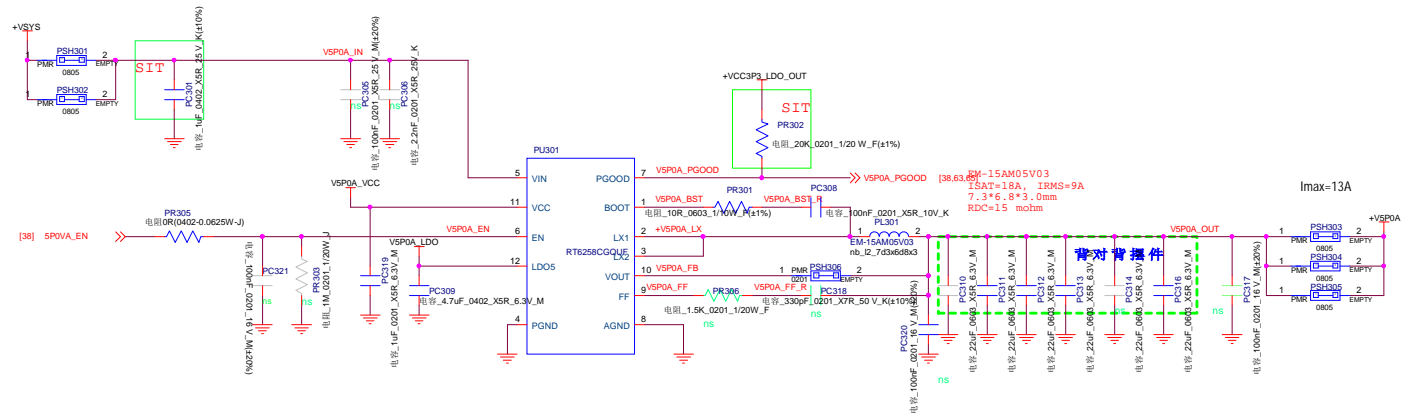


HOLE *14



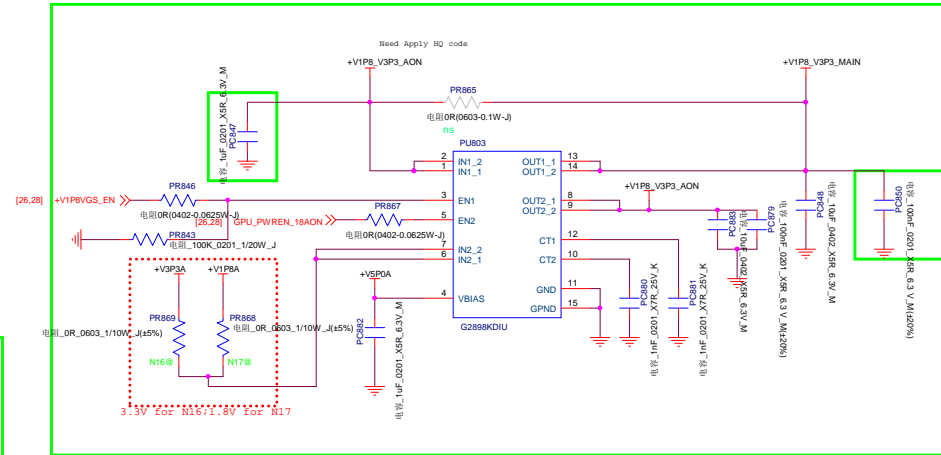
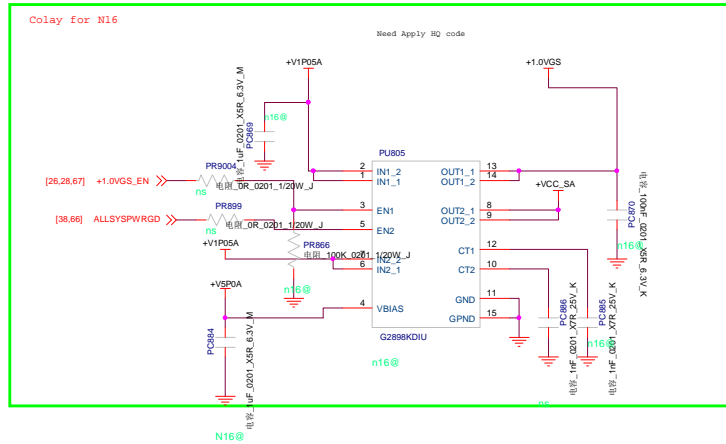
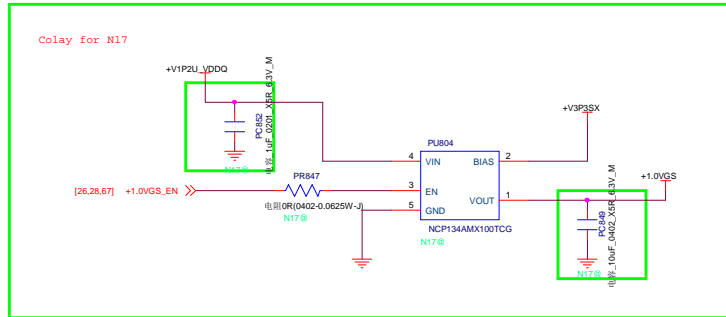
+V1P8A













5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				

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Page name:		BLANK		
Size: A4	Project Name: NB8606			REV: V4.0
Date:		Thursday, July 18, 2019		Sheet: 71 of 72

		Huaqin Telecom Technology Co., Ltd.	
Page name: BLANK			
Size: A4	Project Name: NB8606	REV: V4.0	
Date: Thursday, July 18, 2019	Sheet: 72 of 72		